

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* CHENGFUH JEFFREY TANG and JIANN-TSUEN CHEN

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Appeal 2007-3645  
Application 10/302,489<sup>1</sup>  
Technology Center 2100

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Decided: April 28, 2008

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*Before:* JAMES D. THOMAS, JAY P. LUCAS, and  
ST. JOHN COURTENAY III, *Administrative Patent Judges.*

LUCAS, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF CASE

Appellants appeal from a final rejection of claims 1 to 25 under authority of 35 U.S.C. § 134. The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

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<sup>1</sup> Application filed November 21, 2002. Appellants claims the benefit under 35 U.S.C. § 119 of provisional application 60/631,163, filed 03/01/2002. The real party in interest is the Broadcom Corporation.

Appellants' invention relates to a first in first out (FIFO) buffer circuit for keeping accurate count of the data coming into and out of an electronic buffer before a counter of the data is reset. In the words of the Appellant:

... A method for resetting a gray code counter may include, gradually decrementing or incrementing a write pointer associated with the data buffer unit a reset value of the write pointer is reached in response to an indication that a data buffer controlled by the gray code counter has attained one of a plurality specified states. Additionally, a read pointer associated with the data buffer may be gradually incremented or decremented until a reset value of the read pointer is reached in response to an indication that the data buffer controlled by the gray code counter has attained one of the plurality of specified states. The specified states may include full, empty and one or more predefined states indicating various levels between empty and full. The data buffer may be a first-in-first-out (FIFO) buffer, which may be asynchronously clocked. The data buffer may be adapted to buffer video, voice and/or data.

(Specification, page 4)

Claim 1 is exemplary:

1. A method for resetting a gray code counter, the method comprising:

in response to an indication that a data buffer controlled by the gray code counter has attained one of a plurality specified states, altering gradually, a write pointer associated with said data buffer until a reset value of said write pointer is reached; and

in response to an indication that said data buffer controlled by the gray code counter has attained one of said plurality of specified states, altering gradually, a read pointer associated with said data buffer until a reset value of said read pointer is reached.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

|         |                |               |
|---------|----------------|---------------|
| Ward    | U.S. 5,365,485 | Nov. 15, 1994 |
| Shyi    | U.S. 5,426,756 | Jun. 20, 1995 |
| Watkins | U.S. 4,780,894 | Oct. 25, 1988 |

Applicant Admitted Prior Art (APA); Background of the Invention, pp. 1-3.

Rejections:

- R1: Claims 1 to 3, 5 to 6, 20 to 22 and 24 to 25 stand rejected under 35 U.S.C. § 102(b) for being anticipated by Ward.
- R2: Claims 4 and 23 stand rejected under 35 U.S.C. 103(a) for being obvious over Ward and Admitted Prior Art (APA).
- R3: Claims 7 to 9 and 11 to 13 stand rejected under 35 U.S.C. 103(a) for being obvious over Ward in view of Shyi.
- R4: Claims 14 to 16 and 18 to 19 stand rejected under 35 U.S.C. 103(a) for being obvious over Ward in view of Watkins.

Appellants contend that the claimed subject matter is not anticipated by Ward, or rendered obvious by Ward alone, or in combination with APA, Shyi or Watkins, for reasons to be discussed more fully below. The Examiner contends that each of the claims is properly rejected.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Briefs and the Answer for their respective details. Only those arguments actually made by Appellants have been considered in this opinion. Arguments which Appellants could have made but chose not to

make in the Briefs have not been considered and are deemed to be waived.

*See 37 C.F.R. § 41.37(c)(1)(vii) (2004).*<sup>2</sup>

We affirm the rejections.

### **ISSUE**

The issue is whether Appellants have shown that the Examiner erred in rejecting the claims under 35 U.S.C. §§ 102(b) and 103(a). The issue turns on whether the Ward reference teaches the “altering gradually” limitation as claimed.

### **FINDINGS OF FACTS**

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. Appellants have invented a method for more accurately resetting a gray code counter, specifically one that is used for controlling the reading of data into and the writing of data out of a FIFO data buffer. (Spec. p. 4, ¶ 10 and Figure 3). Usually when writing data, for example a line of video data, into a FIFO buffer, the “write counter” would accurately count the data bits that enter the buffer, and then after the same number of bits is read out of the buffer in accordance with the “read counter” undergo a reset to be placed back into the zero state. (Spec. p. 13, top).

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<sup>2</sup> Appellants have not presented any substantive arguments directed separately to the patentability of the dependent claims or related claims in each group, except as will be noted in this opinion. In the absence of a separate argument with respect to those claims, they stand or fall with the representative independent claim. *See In re Young*, 927 F.2d 588, 590 (Fed. Cir. 1991).

2. Errors sometimes occur in the data feeds or counting, and the reset signal may not be synchronized with the removal of all of the data from the buffer. (Id.) The disclosed invention obviates this error in the following manner:

“On the write side, when a current line of video data has been completely written or the end of current video line is reached, instead of immediately resetting the write pointer 370 to its original starting state, the write pointer may be gradually decremented or incremented until it reaches its starting state. As a result, logic and/or suitable logic in the flag generator block 320 may respond appropriately and no flags may be generated that may indicate an incorrect state of the FIFO buffer 310”. (Spec. p. 13, ¶ [35]).

3. The Ward reference addresses the loading and unloading of FIFO buffers. (Col. 1, l. 52+). It uses gray code counters to keep read and write counts of the data going into and out of the FIFO buffers. (Col. 9, l. 28). To more accurately track the data entering and leaving the buffers, the Ward patent relies on ALMOST FULL and ALMOST EMPTY warning flags, to keep special counts of the critical last stages of filling or emptying the buffer. (Col. 10, ll. 20 to 40). The ALMOST FULL status triggers certain events, such as the “retransmit mode” and the use of temporary storage (shadow storage) to hold overflow or underflow data.

#### **PRINCIPLES OF LAW**

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner’s position. See *In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) (“On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary

indicia of nonobviousness.”) (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. See *In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986) and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984).

Our reviewing court states in *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989) that “claims must be interpreted as broadly as their terms reasonably allow.” Our reviewing court further states that "the words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted). The "ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." (Id. at 1313).

## ANALYSIS

From our review of the administrative record, we find that Examiner has presented a prima facie case for the rejections of Appellants’ claims under 35 U.S.C. §§ 102 and 103. The prima facie case is presented on pages 3 to 14 of the Examiner’s Answer.

In opposition, Appellants present two main arguments. The first argument addresses the issue of whether Ward teaches the “altering gradually” limitation in claim 1, and the other independent claims. In the words of the Appellants, “Ward, however, does not teach, nor suggest, a

method for resetting a gray code counter in which a write pointer associated with a data buffer is altered gradually until a reset value of the write pointer is reached, as recited in claim 1 of the present application.” [emphasis omitted] (Br. p. 10, middle).

Appellants claim, however, is much simpler than Appellants’ argument recited in the quote just above, and can broadly but reasonably read as follows:

“in response to an indication that a data buffer controlled by the gray code counter has attained one of a plurality [of] specified states” is read on Ward buffer states of “not FULL” and thus receptive to receiving written data;

“altering gradually, a write pointer associated with said data buffer until a reset value of said write pointer is reached; and ....” The limitation “gradually” has no specially defined meaning in the Specification, and can be given its ordinary and customary meaning consistent with the Specification. (See *Phillips v. AWH Corp.*, cited above.).

Ward indicates, “Signal WA is simply the output of a Gray-code counter which is set to zero during a FIFO reset and which gets incremented on every FIFO write.” (Col. 9, l. 27). As such we read this steady incrementing of the Gray-code counter as the claimed “altering gradually a write pointer ...” or the “altering gradually, a read pointer” of the next paragraph, and thus find the claimed limitation anticipated by Ward. We understand from the disclosed invention (see FF #2 above) that a more complicated mechanism may occur in the disclosure of the instant invention. However, the claim language is broadly and fairly read on the Ward

reference. The reset value of the write or read pointer is set by the comparators in Ward, fed by the signals from the read and write counters. (Col. 9, ll. 20 to 26). “Gradually” is read on the steady incrementing of the counter as the data is fed to and from the buffer.

With respect to rejection R3, Appellants argue that the reference Shyi does not disclose a prohibition against **attempting** to write to a data buffer or **attempting** to read from a data buffer since it simply disables the write or read action. [emphasis preserved] (Br. p. 18, middle). We have considered the Examiner’s response to this argument (Ans. p. 18, top) and do not find error in it.

As all the claims are subject to the analysis of these two arguments, we do not find error in the rejections applied to each of them, as indicated above in R1 to R4.

### **CONCLUSION OF LAW**

Based on the findings of facts and analysis above, we conclude that the Examiner did not err in rejecting claims 1 to 25.

### **DECISION**

The Examiner's rejection of claims 1 to 25 is affirmed.

AFFIRMED

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