UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte EUGENE D. HAM III

Appeal 2007-3695
Application 09/747,052
Technology Center 2600

Decided: March 21, 2008

Before KENNETH W. HAIRSTON, JOSEPH F. RUGGIERO,
and KEVIN F. TURNER, *Administrative Patent Judges*.

TURNER, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134 from the Examiner's rejection of claims 1-7, 10-16, 18, 24-26, 32-35, 37, and 39. We have jurisdiction under 35 U.S.C. § 6(b). We reverse.

STATEMENT OF CASE

Appellant discloses a system and methods for generating a stable reference clock for carrier frequency generation in communication systems. (Spec. 1: 4-6). The system allows for reduction in clock deviations in the

timing reference signal through the use of a phase-locked loop (PLL) module. (Spec. 2: 7-10).

Claims 1-38 are pending in the application, where claims 8, 9, 17, 19-23, 27-31, 36, and 38 were indicated as containing allowable subject matter. Claims 1-7, 10-16, 18, 24-26, 32-35, 37, and 39 were rejected over prior art in the Final Office Action, but the rejections of claims 5-7, 12-16, 18 and 33 were withdrawn by the Examiner in the Answer. (Ans. 2 and 20). As such, claims 1-4, 10, 11, 24-26, 32, 34, 35, 37, and 39 remain rejected over prior art.

Independent claim 1, which is deemed to be representative, reads as follows:

> 1. A method of generating an output clock signal from a phase-locked loop (PLL), the method comprising:
>
> determining successive phase difference values between a reference clock signal and said output clock signal;
>
> filtering said successive phase difference values to generate successive control values;
>
> controlling a frequency of said output clock signal based on said successive control values; and
>
> adapting a filter used to filter said successive phase difference values based on average control values determined from said successive control values.

The Examiner relies on the following prior art references to show unpatentability:

Glass	US 5,619,543	Apr. 8, 1997

Tanaka	US 5,909,148	Jun. 1, 1999
Wilhelmsson	US 6,353,647 B1	Mar. 5, 2002

Per the rejections that have not been withdrawn, the Examiner rejected claims 1-4, 10, 11, 24-26, 32, and 37 under 35 U.S.C. § 102(b) as being anticipated by Tanaka. The Examiner also rejected claims 34, 35, and 39 under 35 U.S.C. § 103(a) unpatentable over Tanaka and Wilhelmsson.

Rather than repeat the arguments of Appellant or the Examiner, we make reference to the Brief, the Reply Brief and the Answer for their respective details. Only those arguments actually made by Appellant have been considered in this decision. Arguments that Appellant did not make in the Brief have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUE

Has Appellant shown that the Examiner erred in finding claims 1-4, 10, 11, 24-26, 32, 34, 35, 37, and 39 anticipated by Tanaka or obvious by Tanaka and Wilhelmsson?

FINDINGS OF FACT

1. The application details that a PLL includes a controllable oscillator that provides an output signal from the PLL at a frequency proportional to an oscillator control signal from an oscillator controller. The PLL also includes a phase detector which provides a phase error signal by detecting a phase difference between an input clock signal and an output clock signal, and an adjustable loop filter that provides control values based on filtering the phase

error signal. The PLL also includes a control circuit that provides the oscillator control signal responsive to the control values and control logic to control a filter characteristic of the loop filter based on an average control value determined from successive ones of the control values output by the loop filter. (Spec. 9: 5-24; Fig. 5, elements 62, 64, 66, 68, 70, 72, 74, 76 and 78).

2. Independent claim 1 recites, in part, "generating an output clock signal from a phase-locked loop (PLL)," independent claim 10 recites, in part, "controlling a phase-locked loop (PLL) to reduce clock deviations in an output signal," and independent claim 24 recites, in part, "control logic . . . to minimize clock deviations in said output signal."

3. Tanaka discloses a carrier phase synchronizing circuit. A quasi-coherent input signal is provided to the synchronizing circuit and passes through a low pass filter and is introduced to a PLL complex multiplying device. Thereafter, the phase is detected and a demodulated frequency signal is output from the circuit. A portion of the output signal is filtered and is used as an input to a numeric controlling oscillator. The numeric controlling oscillator provides a control value to the PLL complex multiplying device which is proportional to the output frequency. (Abstract; col. 3, l. 42 – col. 4, l. 23; Fig. 1, elements 6 and 8-11).

4. In the Final Office Action, mailed May 10, 2006, the Examiner reconfigured Fig. 1 of Tanaka, as "Figure C," in an attempt to show how an output signal can be derived from the circuit diagram provided in Tanaka. That reconfigured figure, Figure C, is supplied below, as it is addressed in

the Appeal Brief, the Answer and the Reply Brief. (App. Br. 6-8, Ans. 9-11, Reply Br. 3-6).

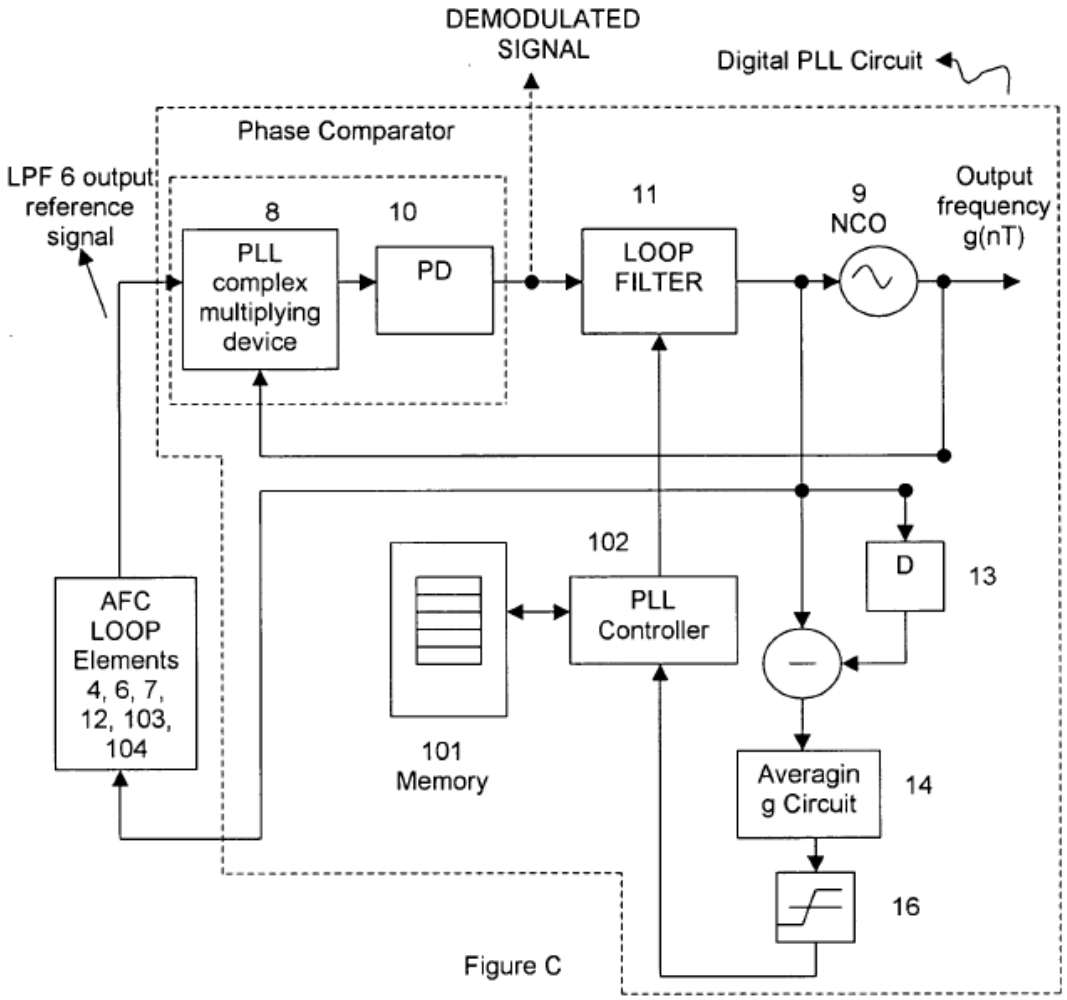

Figure C

Figure C depicts a reconfigured version of a block diagram of a carrier phase synchronizing circuit from Tanaka

5. Wilhelmsson discloses a PLL having very fast acquisition and low output phase jitter and stability. An embodiment of that PLL takes feedback from the output of a digital filter control, which corresponds to a voltage that is beyond the range of a digital-to-analog converter (DAC) and/or the

voltage controlled oscillator (VCO). (Abstract; col. 11, ll. 49-65; Fig. 12, elements 3, 9 and 44).

PRINCIPLES OF LAW

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co. of Calif.*, 814 F.2d 628, 631 (Fed. Cir. 1987). The Examiner bears the initial burden of presenting a prima facie case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). If that burden is met, then the burden shifts to the Appellants to overcome the prima facie case with argument and/or evidence. *See Id*. The analysis need not seek out precise teachings directed to the specific subject matter of the claim but can take into account the inferences and the creative steps that a person of ordinary skill in the art would employ. *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007).

During examination, the claims must be interpreted as broadly as their terms reasonably allow. *In re Am. Acad. of Sci. Tech Center*, 367 F.3d 1359, 1369 (Fed. Cir. 2004). When the specification states the meaning that a term in the claim is intended to have, the claim is examined using that meaning, in order to achieve a complete exploration of the applicant's invention and its relation to the prior art. *In re Zletz*, 893 F.2d 319, 321-22 (Fed. Cir. 1989). The definiteness inquiry focuses on whether those skilled in the art would understand the scope of the claim when the claim is read in light of the rest of the specification. *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576 (Fed. Cir. 1986).

ANALYSIS

Appellant argues that Tanaka fails to disclose a PLL output signal that is generated in a like manner and for a like purpose as disclosed in the Specification and claimed in independent claims 1, 10 and 24. Appellant also argues that the Examiner's position, taken in the rejections, that the claimed PLL output signal and the NCO signal from Tanaka are the same for claim interpretation purposes, as illustrated in Fig. C, is in error. (App. Br. 6-8). We agree with Appellant. The rejection of claims 1, 10 and 24 has been made under 35 U.S.C. § 102(b), and all of the elements of those claims need to be disclosed in Tanaka. All of those claims are concerned with the output clock signal from the phase-locked loop. (Finding of Fact 2). Tanaka fails to disclose such an output clock signal or an equivalent thereof. We find the redrawing of Fig. 1 of Tanaka as Fig. C, (Finding of Fact 4), to show an additional "Output frequency," to be speculative and not supported by the disclosure of Tanaka. While the Examiner is correct that an Output frequency could be obtained from the circuit at that point indicated, there is nothing in Tanaka to suggest such an output, and such a possibility cannot be used to support an anticipation rejection. Thus, we do not find Tanaka to disclose an output clock signal as provided for in independent claims 1, 10 and 24.

The Examiner contends that the Appellant "has confused his own design terms with respect to the **CLOCK OUTPUT** (output of the CO[U]NTER/DIVIDER 78, Fig. 5) and the **output clock signal** (output of Oscillator 74)." (Ans. 9) (emphasis original). The Examiner also contends that the claimed "**output clock signal**" is an "***internal signal to the PLL***

module" and is equivalent to the NCO output signal of Tanaka. (Ans. 10-11) (emphasis original). Appellant argues that such a finding by the Examiner is contradicted by the language of the Specification and the claims. (Reply Br. 4). As Appellant has indicated, the Specification makes clear that the oscillator (74) generates the output clock, (Spec. 9: 16-17), which is the output signal of the PLL module. The fact that the output of the oscillator may also be an "internal" signal is immaterial because we are concerned with the output clock signal, as recited in the independent claims. Indeed, any signal output from a module would necessarily be an internal signal, at some point, if that module has any function. As such, we do not find the Examiner's contentions about the similarity of the claimed signals and the signal in Tanaka to be compelling.

While Appellant has raised additional arguments with respect to the rejections of independent claims 1, 10 and 24, and claims dependent thereon, we need not discuss those arguments because we find that Tanaka fails to disclose an output clock signal as recited in the independent claims. As such, we find the rejection of claims 1-4, 10, 11, 24-26, 32 and 37 was made in error. Additionally, with respect to the rejection of claims 34, 35 and 39, we find that Wilhelmsson fails to cure the above-discussed deficiencies of Tanaka, and we find that rejection of claims 34, 35 and 39 to be improper because of the dependency of those claims on independent claim 24.

CONCLUSION OF LAW

We find that the Examiner erred in rejecting claims 1-4, 10, 11, 24-26, 32, 34, 35, 37 and 39 under 35 U.S.C. §§ 102 and 103 based on Tanaka or Tanaka and Wilhelmsson.

DECISION

The rejections of claims 1-4, 10, 11, 24-26, 32, 34, 35, 37 and 39 are reversed. The rejections of claims 5-7, 12-16, 18 and 33 were withdrawn by the Examiner.

REVERSED

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