

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* SHER JIUN FANG, SEE TAUR LEE, and  
ABDELLATIF BELLAOUAR

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Appeal 2007-3810  
Application 10/227,937<sup>1</sup>  
Technology Center 2800

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Decided: November 28, 2007

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Before JOSEPH L. DIXON, JAY P. LUCAS, and SCOTT R. BOALICK,  
*Administrative Patent Judges.*

BOALICK, *Administrative Patent Judge.*

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1-8, all the claims pending in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

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<sup>1</sup> Application filed August 26, 2002. The real party in interest is Texas Instruments Incorporated.

## STATEMENT OF THE CASE

Appellants' invention relates to a differential Complementary Metal Oxide Semiconductor (CMOS) latch and a digital quadrature generator using the CMOS latch. (Spec. 1:7-9.)

Claim 1 is exemplary:

1. A first differential Clocked-CMOS ( $C^2MOS$ ) latch, comprising:

first (CLK) and second (CLKb) clock input ports for receiving complementary clock signals (CLOCK and CLOCKb);

first and second input ports (D and Db);

first and second output ports (Q and Qb);

a pair of back-to-back inverters coupled between the first and second output ports; and

a second differential Clocked-CMOS ( $C^2MOS$ ) latch, comprising:

third (CLK\_1) and fourth (CLKb\_1) clock input ports for receiving complementary clock signals (CLOCK 1 and CLOCKb 1);

third and fourth input ports (D1 and Db1);

third and fourth output ports (Q1 and Qb1);

a second pair of back-to-back inverters coupled between the third and fourth output ports,

wherein said first and second differential clocked-CMOS latches are connected in a master-slave relationship.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Boerstler                    US 6,507,228 B2                    Jan. 14, 2003

Admitted Prior Art, Fig. 1 in the present application (APA).

Claims 1-8 stand rejected under 35 U.S.C. § 103(a) as being obvious over the APA and Boerstler.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Brief and the Answer for their respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments that Appellants did not make in the Brief have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2004).<sup>2</sup>

## ISSUE

The issue is whether Appellants have shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 103(a). The issue turns on whether

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<sup>2</sup> Except as will be noted in this opinion, Appellants have not presented any substantive arguments directed separately to the patentability of the dependent claims or related claims in each group. In the absence of a separate argument with respect to those claims, they stand or fall with the representative independent claim. *See* 37 C.F.R. § 41.37(c)(1)(vii).

the APA and Boerstler teach or suggest each and every limitation of the claims.

#### FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. The APA teaches a circuit with two differential latches connected in a master-slave relationship. (Spec. Fig. 1.) The latches are source coupled logic latches. (Spec. 1:14-20; Fig. 1.)
2. Boerstler teaches clocked latches in electronic circuitry which are suitable for use with a high frequency clock. (Col. 1, ll. 20-22.)  
Boerstler teaches a clocked CMOS latch 400 that one of ordinary skill in the art would recognize as a differential Clocked-CMOS (C<sup>2</sup>MOS) latch. (Fig. 4; col. 6, l. 54 to col. 7, l. 6; *see also* Figs. 1, 3.) The memory cell 140 of latch 400 is a pair of back-to-back inverters Q16 and Q17. (Col. 3, ll. 17-20.)

#### PRINCIPLES OF LAW

All timely filed evidence and properly presented arguments are considered by the Board in resolving an obviousness issue on appeal. *See In re Piasecki*, 745 F.2d 1468, 1472 (Fed. Cir. 1984).

In the examination of a patent application, the Examiner bears the initial burden of showing a *prima facie* case of unpatentability. *Id.* at 1472. When that burden is met, the burden then shifts to the applicant to rebut. *Id.*; *see also In re Harris*, 409 F.3d 1339, 1343-44 (Fed. Cir. 2005) (finding

rebuttal evidence unpersuasive). If the applicant produces rebuttal evidence of adequate weight, the prima facie case of unpatentability is dissipated. *In re Piasecki*, 745 F.2d at 1472. Thereafter, patentability is determined in view of the entire record. *Id.*

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1734 (2007). In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," *id.* at 1739, and reaffirmed principles based on its precedent that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results," *id.*

## ANALYSIS

Appellants contend that Examiner erred in rejecting claims 1-8 as being obvious over the APA and Boerstler. Reviewing the documents of record and the findings of facts cited above, we do not agree. In particular, we find that the Appellants have not shown that the Examiner failed to make a prima facie showing of obviousness with respect to claims 1-8. Appellants failed to meet the burden of overcoming that prima facie showing.

Regarding claim 1, Appellants argue that neither the APA nor Boerstler "disclose or suggest the presently claimed invention including the first and second clock CMOS latch connected in a master-slave relationship." (Br. 3-4.) We do not agree.

The Examiner found that the APA meets all the limitations of claim 1 except that the APA uses source coupled logic latches rather than differential Clocked-CMOS (C<sup>2</sup>MOS) latches. (Ans. 3-4; *see also* FF 1.) In addition, the Examiner found that Boerstler teaches a C<sup>2</sup>MOS latch (Ans. 3-5; FF 2) and found that one of ordinary skill in the art would have replaced the source coupled logic latches of the APA with the C<sup>2</sup>MOS latches of Boerstler (Ans. 3-5). Boerstler's teachings are in the same field of endeavor as the APA, and the substitution of the more modern C<sup>2</sup>MOS latches was within the ordinary skill of the practitioner, with no unexpected results. Thus, we agree with the finding of the Examiner.

Claims 2-8 were not argued separately, and fall together with claim 1.

Accordingly, we conclude that the Examiner did not err in rejecting claims 1-8 under 35 U.S.C. § 103(a).

#### CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that the Examiner did not err in rejecting claims 1-8.

#### DECISION

The rejection of claims 1-8 for obviousness under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

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AFFIRMED

tdl/gvw

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