UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TRENT LORNE MCCONAGHY

Appeal 2007-3818
Application 10/337,271
Technology Center 2800

Decided: August 19, 2008

Before KENNETH W. HAIRSTON, JOSEPH F. RUGGIERO and JOHN A. JEFFERY, *Administrative Patent Judges*.

HAIRSTON, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134 from a final rejection of claims 1 to 5, 8, 9, 11 to 14, and 16 to 18. After submission of the brief, the Examiner maintained the rejection of claims 1 to 5, 8, 9, and 11 to 13. We have jurisdiction under 35 U.S.C. § 6(b).

We will sustain the rejection.

Appellant has invented a system for electronic circuit design that applies an optimization process to direct representations of circuit design candidates to alter the direct representations to determine at least one optimized circuit design candidate (Figure 5; Spec. 4, 5, 9, and 11 to 13).

Claim 1 is the only independent claim on appeal, and it reads as follows:

1. A system for electronic circuit design comprising:

storage means for storing direct representations of circuit design candidates;

a storage means interface for changing the direct representations of the circuit design candidates in the storage means;

an optimizer for applying an optimization process to the direct representations to determine at least one optimized circuit design candidate, the optimizer being capable of altering the direct representations by interacting with the storage means interface; and

a user interface for allowing user manipulation of the direct representations during the optimization process by interacting with the storage means interface.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Garnett	US 6,516,456 B1	Feb. 4, 2003 (filed Jan. 27, 1997)

The Examiner rejected claims 1 to 5, 8, 9, and 11 to 13 under 35 U.S.C. § 102(e) based upon the teachings of Garnett.

ISSUE

Appellant contends *inter alia* that Garnett does not describe an electronic circuit design system that includes an optimizer and a user interface as set forth in the claims on appeal (App. Br. 14). Thus, the issue before is does the Garnett electronic circuit design system describe an optimizer and a user interface as set forth in the claims on appeal?

FINDINGS OF FACT

1. As indicated *supra*, Appellant describes and claims a system for electronic circuit design that uses an optimization process to alter direct representations of circuit design candidates to determine at least one optimized circuit design candidate.

2. Garnett describes an electronic design automation (EDA)[1] system 12 for electronic circuit design (Fig. 1; col. 1, ll. 52 to 54). The electronic circuit design system includes a storage means (i.e., circuit design database 20) (Fig. 2; col. 9, ll. 39 to 41; col. 10, ll. 55 to 64) for storing direct representations (col. 5, ll. 27 and 28; col. 9, ll. 39 to 41; col. 22, l. 67 to col. 23, l. 1). The system described by Garnett uses a database editor tool as an interface to the circuit design database storage means to change/edit the direct representations of the circuit design candidates in the storage means (col. 5, ll. 22 to 30; col. 9, ll. 2 to 6). Garnett uses an optimizer that interacts with the storage means interface to apply an optimization process to the direct representations to alter the direct representations to thereby determine

[1] According to Appellant, "[t]he present invention relates to electronic design automation (EDA), particularly the field of analog and mixed-signal (AMS) circuit design" (Spec. 1).

at least one optimized circuit design candidate (col. 3, ll. 26 to 31; col. 9, ll. 39 to 48; col. 10, ll. 18 to 41; col. 11, ll. 7 to 53). In the Garnett system, the user interface for allowing user manipulation of the direct representations of circuit design candidates can be an input device 16 (e.g., a mouse and a keyboard) and a display 18 (col. 9, ll. 19 to 33).

PRINCIPLES OF LAW

Anticipation is established when a single prior art reference discloses expressly or under the principles of inherency each and every limitation of the claimed invention. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1347 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79 (Fed. Cir. 1994).

ANALYSIS

As indicated *supra* in finding of fact 2, Garnett clearly describes an electronic circuit design system that includes a storage means, a storage means interface, an optimizer, and a user interface as set forth in claim 1 and the claims that depend therefrom. With respect to claims 2 and 12, the keyboard, mouse, and display create an interactive user display interface for the circuit designer to view and edit the circuit design representations. As indicated *supra* in finding of fact 2, Garnett describes a database interface as set forth in claim 3. The finding of fact 2 makes clear that the user can edit a representation of a circuit design during the optimization process as required by claims 4, 5, 8, 9, and 11. As indicated *supra* in footnote 1, the EDA system described by Garnett encompasses analog and mixed-signal (AMS)

circuit design as required by claim 13. Thus, Appellant's arguments that Garnett fails to describe the claimed electronic circuit design structure are without merit (App. Br. 13 to 16; Reply Br. 3 to 6).

In summary, we agree with the Examiner that the anticipation rejection is proper because Garnett describes all of the system structure set forth in claims 1 to 5, 8, 9, and 11 to 13 on appeal.

CONCLUSION OF LAW

Anticipation has been established by the Examiner because Garnett does disclose each and every limitation of the claimed invention set forth in claims 1 to 5, 8, 9, and 11 to 13.

ORDER

The anticipation rejection of claims 1 to 5, 8, 9, and 11 to 13 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

KIS

BEVER, HOFFMAN & HARMS, L.L.P.
2099 GATEWAY PLACE
SUITE 320
SAN JOSE, CA 95110