

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ROY E. SCHEUERLEIN

Appeal 2007-4129
Application 10/253,024
Technology Center 2800

Decided: April 8, 2008

Before ANITA PELLMAN GROSS, MAHSHID D. SAADAT,
and KEVIN F. TURNER, *Administrative Patent Judges*.

GROSS, *Administrative Patent Judge*.

DECISION ON APPEAL
STATEMENT OF THE CASE

Scheuerlein (Appellant) appeals under 35 U.S.C. § 134 from the Examiner's Final Rejection of claims 1 through 7, 9, 10, 12, 13, and 16 through 20. We have jurisdiction under 35 U.S.C. § 6(b).

Appellant's invention relates to a method of sensing the data state of a selected memory cell in a memory array having two or more planes of

memory cells. *See generally* Spec. 3, paragraphs [1009]-[1010]. Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. In a memory array having at least two memory planes of memory cells with diode-like conduction characteristics, for at least one of two memory cell data states, each memory cell within a memory plane coupled between a word line and a bit line associated with the memory plane and having first and second nominal current levels in accordance with its data state when forward biased, a method of sensing the data state of a selected memory cell comprising the steps of:

driving a selected word line from an unselected word line bias voltage to a selected word line bias voltage;

driving a selected bit line from an unselected bit line bias voltage to a selected bit line bias voltage; and

sensing current flow on the selected bit line while the selected bit line remains substantially at the selected bit line bias voltage to determine which of the first or second nominal current levels flows through the selected memory cell.

The prior art references of record relied upon by the Examiner in rejecting the appealed claims are:

Johnson	US 6,034,882	Mar. 07, 2000
Scheuerlein	US 6,130,835	Oct. 10, 2000
Cho	US 6,400,606 B1	Jun. 04, 2002

Claims 1 through 7, 9, 10, and 12 stand rejected under 35 U.S.C. § 103 as being unpatentable over Scheuerlein in view of Johnson.

Claims 13 and 16 through 20 stand rejected under 35 U.S.C. § 103 as being unpatentable over Scheuerlein in view of Johnson and Cho.

We refer to the Examiner's Answer (mailed March 5, 2007) and to Appellant's Brief (filed May 31, 2005) and Reply Brief (filed October 24, 2005) for the respective arguments.

SUMMARY OF DECISION

As a consequence of our review, we will affirm the obviousness rejection of claims 1 through 7, 9, 10, and 12 but reverse the obviousness rejection of claims 13 and 16 through 20.

OPINION

The Examiner asserts (Ans. 4-5) that Scheuerlein discloses all of the steps of claim 1, but "does not disclose that the memory array is a multi-level array having more than one plane of memory cells." The Examiner asserts (Ans. 5) that Johnson discloses that using multiple memory planes maximizes the array efficiency, and, therefore, that it would have been obvious to include multiple memory planes in Scheuerlein.

Appellant does not argue any of the teachings of Scheuerlein asserted by the Examiner. Appellant only contests the combination of Scheuerlein with Johnson's multiple planes. Specifically, Appellant contends (App. Br. 5-7) that the statement in Johnson relied upon for motivation to combine with Scheuerlein has nothing to do with using multiple memory planes. Further, since Scheuerlein's and Johnson's memory cells are different, according to Appellant, there is no motivation to combine Johnson's multiple memory planes with Scheuerlein's memory cells. The issue, therefore, is whether it would have been obvious in view of Scheuerlein and Johnson to use multiple memory planes for Scheuerlein's memory cells.

Scheuerlein suggests (col. 2, ll. 38-39) that an increase in the number of memory cells is needed "for the cross point array of FIG. 1 to have a useful number of memory cells." Johnson states (col. 1, ll. 14-19) that higher density semiconductor memories are needed and (col. 4, ll. 17-19) that multiple layers of memory cells provide high density. Although we recognize that Johnson's memory cells differ from Scheuerlein's, we find the teaching in Johnson to use multiple layers for higher density arrays to be more of a general teaching rather than limited to the particular types of memory cells disclosed by Johnson. Further, Johnson's Figures 10(a) and 10(b), which show multiple layers of cells, show generic memory cells, thereby bolstering the case of a generic teaching.

We note also that the Supreme Court has held that in analyzing the obviousness of combining elements, a court need not find specific teachings, but rather may consider "the background knowledge possessed by a person having ordinary skill in the art" and "the inferences and creative steps that a person of ordinary skill in the art would employ." *See KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1740-41 (2007). To be nonobvious, an improvement must be "more than the predictable use of prior art elements according to their established functions," and the basis for an obviousness rejection must include an "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Id.* Johnson actually teaches that using multiple layers provides higher density. We find that using multiple layers in Scheuerlein is no more than the predictable use of a prior art element according to its established function of providing higher density. Therefore, we will sustain the obviousness rejection of claims 1 through 7, 9, 10, and 12 over Scheuerlein and Johnson.

For claims 13 and 16 through 20, the Examiner (Ans. 6-7) adds Cho to the primary combination for a suggestion to sense current flow by "subtracting a reference current having a magnitude between the first and second nominal current levels from the bit line current, resulting in a net bit line current; and sensing whether the net bit line current is positive or negative," as recited in claim 13. The Examiner asserts (Ans. 6) that Cho's differential amplifier inherently senses whether the net bit line voltage is positive or negative and "a ordinary practitioner would know that comparing input voltages is inherently comparing input currents because Ohm's law, which is a basic postulate of circuit theory states that $V = I \cdot R$ (or $I = V/R$).". Further, the Examiner asserts (Ans. 7) that it would have been obvious to apply Cho's method of sensing memory cell current "because it is one of the common methods for reading memory cells."

Appellant contends (App. Br. 8) that the Examiner's characterization of Cho is incorrect. Specifically, Appellant contends that Cho's net bit line adopts a voltage between V_{CC} and ground, not between a positive and a negative voltage. Further, Appellant contends (App. Br. 8) that Cho does not disclose "'*subtracting* a reference current having a magnitude between the first and second nominal current levels from the bit line current'" nor does Cho sense whether a "'*net* bit line current'" is positive or negative. Instead Cho discloses a differential amplifier that finds a difference between two input voltages. *See* App. Br. 9. Accordingly, Appellant contends (App. Br. 10) that the Examiner has failed to establish a prima facie case of obviousness for claims 13 and 16 through 20. The issue, therefore, is whether Cho, in combination with Scheuerlein and Johnson would have led

the skilled artisan to the method of sensing current flow as recited in claim 13. We agree with Appellant that it would not.

Cho's differential amplifier 118, as pointed out by Appellant, senses a difference, but not the particular difference (a net bit line current) recited in claim 13. Comparing input voltages is not inherently the same as comparing input currents, and we find no suggestion in Cho to compare input currents. Further, even if we accepted the Examiner's characterization of Cho's teachings, we find no rationale in Cho for sensing current as recited in claim 13 in Scheuerlein. Consequently, we cannot sustain the obviousness rejection of claims 13 and 16 through 20 over Scheuerlein, Johnson, and Cho.

ORDER

The decision of the Examiner rejecting claims 1 through 7, 9, 10, 12, 13, and 16 through 20 under 35 U.S.C. § 103 is affirmed as to claims 1 through 7, 9, 10, and 12 but reversed as to claims 13 and 16 through 20.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a). *See* 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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