UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KIEN BENG TAN

Appeal 2008-0033
Application 10/319,391
Technology Center 2800

Decided: January 28, 2008

Before KENNETH W. HAIRSTON, SCOTT R. BOALICK, and JOHN A. JEFFERY, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134 from the Examiner's rejection of claims 1-52. We have jurisdiction under 35 U.S.C. § 6(b), and we heard the appeal on January 22, 2008. We affirm-in-part.

STATEMENT OF THE CASE

Appellant invented a preamplifier integrated circuit device for a magnetic storage device that includes multiple channels and one or more interconnecting layers. A passivation layer is arranged adjacent to the interconnecting layers and external connections are arranged in openings in the passivation layer. The external connections independently communicate with each group of channels. Such an arrangement simplifies power distribution and reduces heating as the number of read and write channels increase.[1] Claim 1 is illustrative:

1. A preamplifier integrated circuit (IC) for a magnetic storage device comprising:

a plurality of channels, each including at least one preamplifier;

one or more interconnecting layers;

a passivation layer arranged adjacent to said interconnecting layers; and

a plurality of first external connections that are arranged in openings in said passivation layer, that are in contact with at least one of said interconnecting layers and that are adapted to distribute a first potential to said preamplifiers,

wherein said plurality of channels are arranged in a plurality of groups, each of said plurality of groups includes at least one of said channels,

wherein at least one of said first external connections independently communicates with each of said groups, and

[1] *See generally* Spec. ¶¶ 0001, 0010-18.

wherein the first potential is distributed to a respective one of said plurality of groups via the corresponding at least one of said external connections.

The Examiner relies on the following prior art references to show unpatentability:

Kawahara	US 5,300,839	Apr. 5, 1994
Smith	US 5,744,898	Apr. 28, 1998
Henrichs	US 6,249,824 B1	Jun. 19, 2001

1. Claims 1-26 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Henrichs and Smith.[2]
2. Claims 27-52 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Kawahara and Smith.

Rather than repeat the arguments of Appellant or the Examiner, we refer to the Briefs[3] and the Answer for their respective details. In this decision, we have considered only those arguments actually made by Appellant. Arguments which Appellant could have made but did not make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

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[2] The Examiner withdrew a previous objection to claims 1-26 (Ans. 11). Nonetheless, such an issue would not be before us in any event as objections are petitionable matters -- not appealable matters. *See* MPEP § 706.01 ("[T]he Board will not hear or decide issues pertaining to objections and formal matters which are not properly before the Board."); *see also* MPEP § 1201 ("The Board will not ordinarily hear a question that should be decided by the Director on petition….").

[3] We refer to the most recent Appeal Brief filed August 30, 2005 and the Reply Brief filed January 6, 2006 throughout this opinion.

OPINION

The Rejection of Claims 1-26

Independent Claims 1 and 12

We first consider the Examiner's rejection of claims 1-26 under 35 U.S.C. § 103(a) as unpatentable over Henrichs and Smith. In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966).

Discussing the question of obviousness of a patent that claims a combination of known elements, *KSR Int'l v. Teleflex, Inc*., 127 S. Ct. 1727 (2007), explains:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida* [*v. AG Pro, Inc.,* 425 U.S. 273 (1976)] and *Anderson's-Black Rock*[*, Inc. v. Pavement Salvage Co*., 396 U.S. 57 (1969)] are illustrative—a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

KSR, 127 S. Ct. at 1740. If the claimed subject matter cannot be fairly characterized as involving the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art

ready for the improvement, a holding of obviousness can be based on a showing that "there was an apparent reason to combine the known elements in the fashion claimed." *Id*. at 1740-41. Such a showing requires "some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id*. at 1741 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

If the Examiner's burden is met, the burden then shifts to the Appellant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. *See In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

Regarding independent claims 1 and 12, the Examiner's rejection essentially finds that Henrichs teaches a preamplifier IC for a magnetic storage device with every claimed feature except for arranging plural first external connections in openings in a passivation layer. The Examiner, however, notes that passivation layers are known in the art as evidenced by Appellant's Specification (Spec. ¶ 0008). The Examiner further notes that external connections such as power and signals conventionally communicate with a chip through openings in the passivation layer. Additionally, the Examiner indicates that external connections are likewise formed in Henrichs' device to provide power and signals to the chip (Ans. 4-5).

Alternatively, the Examiner cites Smith for teaching arranging multiple external connections in openings in a "passivation layer" MLC (Ans. 5).

In view of these teachings, the Examiner concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to arrange plural first external connections in openings in a passivation layer of Henrichs' device (Ans. 5).

Regarding representative claim 1,[4] Appellant argues that the prior art does not teach nor suggest (1) a preamplifier IC that *independently* supplies a first potential via external connections and interconnecting layers to each group, or (2) a passivation layer with openings for receiving the external connections as claimed (App. Br. 7-9; Reply Br. 4, 9-12). Appellant contends that the identified teachings in Henrichs were taken out of context and the references are not properly combinable (App. Br. 8-9). According to Appellant, since all of the address circuits in Figures 71A and 75 of Henrichs are all supplied by the same voltage line through a single external connection to the IC, this arrangement actually teaches away from the claimed preamplifier IC layout (App. Br. 10; Reply Br. 10). Appellant adds that the read and write preamplifier circuits of the microhead array chip in Henrichs likewise teach away from the recited IC layout since these circuits are all supplied by the same voltage line through a single external connection (Reply Br. 10).

[4] Appellant argues independent claims 1 and 12 together as a group. *See* App. Br., at 7; *see also* Reply Br., at 4, 9. Accordingly, we select claim 1 as representative. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Appellant also argues that Smith -- a reference disclosing an ultrasound transducer array -- does not cure the deficiencies of Henrichs. Appellant emphasizes that Smith does not discuss passivation or interconnecting layers, let alone arranging plural external connections in a passivation layer where at least one of the external connections independently communicates with each of the groups as claimed (App. Br. 10; Reply Br. 12).

In addition, Appellant argues that Smith is non-analogous art. In reaching this conclusion, Appellant contends that Smith is neither in the field of Appellant's endeavor (preamplifier ICs for magnetic media storing devices) nor is the reference reasonably pertinent to the particular problem with which Appellant is involved (App. Br. 10-12; Reply Br. 13-14).

The Examiner notes that the claim language merely requires only one external connection to independently communicate with each group -- a limitation that is fully met by the VDD or GND contacts in Henrichs (Ans. 12, 16-17). The Examiner adds that while the various figures from Henrichs that were relied upon pertain to different aspects of Henrichs' device, they all nonetheless are part of the magnetic micro-head array chip (Ans. 13). In addition, although the Examiner acknowledges that Henrichs does not explicitly state that a passivation layer is used, the Examiner reiterates that such a layer is known in the art as evidenced by Appellant's Specification and, in any event, would have been obvious in view of Smith (Ans. 14). Regarding Smith, the Examiner asserts that skilled artisans would use a "voltage supply/protection structure" such as that disclosed by Smith in Henrichs' IC device (Ans. 17-18).

The issue before us, then, is whether Henrichs, considered with either (1) the admitted prior art disclosed in the Specification, or (2) the disclosure of Smith, reasonably teaches or suggests the limitations of representative claim 1. For the reasons that follow, we find that Henrichs considered with the admitted prior art does, in fact, reasonably suggest the limitations of representative claim 1. However, Henrichs considered with Smith does not.

Henrichs discloses a magnetic data storage fixed hard disk drive that uses stationary Microhead Array Chips (MACs). The MACs are mounted on chip-positioning circuit boards 27 adjacent to the hard disk's data storage platter 13 (Henrichs, col. 1, ll. 34-43; col. 25, ll. 16-18; Fig. 1).

Every MAC has a group of 64 circuit contacts physically embedded into the bottom surface of the chip's outer shell. These embedded contacts correspond to matching contacts embedded into the top surface of the circuit board's chip socket (Henrichs, col. 42, ll. 31-42; Figs. 11, 12, 26-27, 30, 32, 35, 37). As best seen in Figures 11 and 12, the MAC's contacts include, among other things, +5V and GND connections (connections 33 and 34).

Figure 65A details the MAC's functionality.[5] As shown in that figure, the MAC includes, among other things, two distinct read and write preamp circuits. The GND and +5V connections of each preamp circuit are each connected to the GND and +5V contacts of the MAC, respectively (Henrichs, Figs. 65A, 65C, 65D).

[5] Although we discuss the embodiment of Figure 65A which details one type of MAC (i.e., a magnetoresistor MAC), Figure 64A likewise shows commensurate features relevant to this appeal for a different type of MAC (i.e., magnetic MAC). *See* Henrichs, at col. 45, ll. 41-50 (distinguishing the two MAC design strategies).

In our view, these teachings from Henrichs reasonably suggest several key features of representative claim 1. First, we find the read and write signal flow paths shown in Figure 65A are arranged in two groups of channels each with an associated preamplifier.[6] Second, we find that the GND and +5V contacts of the MAC reasonably correspond to plural "first external connections" as they distribute a potential (+5V or GND) to the read and write preamplifier circuits, respectively. Third, we find that both the +5V and the GND contacts independently communicate with each of the groups. As shown in Figures 65A, 65C, and 65D, there are at least two independent and distinct conductive lines that extend from the MAC's +5V and the GND connections to the read and write preamplifier circuits, respectively. That is, there are independent connections between either the +5V or the GND contacts and the respective read and write preamplifiers.

Appellant's argument that Henrichs teaches away from the claimed invention since Henrichs' read and write preamplifiers are all supplied by the same voltage through a single external connection (Reply Br. 10) is unavailing and, in any event, not commensurate with the scope of the claim language. Both the +5V or the GND contacts constitute external connections with respect to the MAC. Moreover, these external connections distribute at least one potential to the respective groups as noted above.

Based on these findings in Henrichs, we now address the differences between Henrichs and the claimed invention and whether such differences would have been obvious to the ordinarily skilled artisan in light of the cited

[6] *See also* Henrichs, at col. 14, ll. 29-30 (referring to the MAC's preamplifiers as a "Read Channel Preamp" and a "Write Channel Preamp" respectively).

prior art. At the outset, we note that Henrichs teaches the MAC's read and write microhead arrays along with their control, switching, addressing, *amplifying*, encoding, and decoding circuitry is fabricated as a single CMOS MAC device using standard CMOS photo-resist oxide masking, etching, and layer techniques (Henrichs, col. 14, ll. 13-36; emphasis added). Henrichs, however, does not provide any specific structural details of this integrated CMOS structure apart from a discussion of the multi-layer CMOS fabrication techniques employed for the various components of the device.[7]

In the Background section of the Specification, Appellant notes that preamplifier ICs are typically formed on wafers by repeated film deposition, masking, etching, and doping techniques until the individual devices of each preamplifier are formed. Then, the individual devices are interconnected using one or more metal layers separated by insulating layers. Vias interconnect the separated metal layers. In addition, a passivation layer is typically deposited to protect the IC from damage and/or contamination.

[7] Although the Examiner refers to the formation of an oxide layer in connection with these manufacturing techniques (Ans. 14), the cited passages merely refer to fabricating the *Induction Channel Coils* of the MAC (Henrichs, col. 12, l. 50 - col. 13, l. 2). Nevertheless, Henrichs does indicate that commensurate multi-layer CMOS fabrication techniques can be used for other components of the MAC, namely the MAC's Yoke Cores, Magnetic Flux Concentration Tips, and Magnetoresistor read elements (Henrichs, col. 13, l. 3 - col. 14, l. 12). Even if we assume, without deciding, that the oxide layers used in this fabrication process are merely temporary masking agents as Appellant alleges (Reply Br. 11), we disagree with Appellant's assertion that these fabrication techniques are "wholly irrelevant." On the contrary, while Henrichs does not provide specific details regarding the internal structure of the MAC, the fabrication techniques described in Henrichs nonetheless suggest that the MAC is a multi-layered CMOS structure.

Openings are formed in the passivation layer to allow electrical contact to be made with the metal layers using solder bumps and traces on the flex circuit (Spec. ¶ 0008).

According to the Specification, power supply voltages are typically delivered to the preamplifier IC using a trace and solder bump. After reaching the IC, power is distributed in the metal layers of the IC (Spec. ¶ 0009).

This admitted prior art discussion amply teaches that passivation and interconnecting layers are well known in preamplifier ICs. Moreover, this discussion evidences that it is well known to form openings in the passivation layer to allow electrical contact to be made with the interconnecting layers.

Therefore, in our view, there is ample suggestion on this record to provide a passivation layer adjacent to interconnecting layers in the MAC device of Henrichs to, among other things, protect the IC from contamination and distribute power via internal conductive layers. We reach this conclusion mindful that Henrichs strongly suggests that the MAC is a multi-layer CMOS device as we noted previously.[8] Furthermore, based on these collective teachings, ordinarily skilled artisans would readily recognize that the external connections of the MAC would be arranged in openings of the passivation layer to enable electrical contact with the connections.

For the foregoing reasons, we will sustain the Examiner's rejection of representative claim 1 based on the collective teachings of Henrichs and the admitted prior art in the Specification. We will also sustain the Examiner's rejection of claim 12 which falls with claim 1.

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[8] *See* p. 10 n.7, *supra*, of this opinion.

However, we find the Examiner's reliance on Smith unavailing essentially for the reasons indicated by Appellant. Smith discloses an ultrasound transducer array with integrated transmitter and receiver circuitry for generating and receiving ultrasonic pulses (Smith, Abstract). In Figure 17, transmitter and receiver ICs are disposed in a recess 870. Transmit and receive element connections are routed through a multilayer ceramic (MLC) connector 850 to a quarter wave mismatching layer 840 and multilayer piezoelectric material 820 disposed thereabove (Smith, col. 18, l. 33 - col. 19, l. 35; Figs. 17-18B).

At best, Smith merely teaches providing electrical connections to and from the ICs in a multilayer ceramic connector. But to assert that this very limited teaching would somehow suggest providing a passivation layer in the MAC of Henrichs, let alone disposing the MAC's external connections in openings in such a passivation layer, simply strains reasonable limits and is tantamount to hindsight reconstruction of the invention. Moreover, we agree with Appellant that Smith is not in the same field of endeavor as Appellant's invention. Nor do we find that Smith's transducer arrangement is reasonably pertinent to the problem that Appellant is trying to solve. The specific structural arrangement in Figure 17 is for an entirely different purpose and functions in an entirely different manner. Therefore, we cannot sustain the Examiner's rejection of claims 1-26 based on Henrichs and Smith.

Dependent Claims 2-11 and 13-26

Although Appellant nominally argues the rejection of dependent claims 2-11 and 13-26 separately (App. Br. 12; Reply Br. 15), the arguments

presented do not separately point out with particularity or explain why the limitations of the dependent claims are separately patentable. Rather, Appellant merely asserts patentability of the claims for the same reasons advanced in connection with the independent claims and summarily alleges patentability of the dependent claims "to the extent they mention further aspects of the preamplifier IC" (*Id.*). Since Appellant has not persuasively rebutted the Examiner's prima facie case of obviousness for dependent claims 2-11 and 13-26 based on the collective teachings of Henrichs and the admitted prior art, we will sustain the rejection of claims 2-11 and 13-26 for the same reasons discussed above with respect to claims 1 and 12.

The Rejection of Claims 27-52

We now consider the Examiner's rejection of claims 27-52 under 35 U.S.C. § 103(a) as unpatentable over Kawahara and Smith. The Examiner finds that Kawahara teaches a preamplifier IC with every claimed feature except for arranging plural first external connections in a passivation layer on a substrate including a first trace. The Examiner again cites Figure 17 of Smith and concludes that arranging plural first external connections via a passivation layer and solder ball arrangement would have been obvious to one of ordinary skill in the art (Ans. 7-9).

Regarding independent claims 27 and 40, Appellant argues that the signals relied upon by the Examiner in Kawahara are all different signals which are not equivalent to the recited potential that must be independently distributed to all of the groups and at least one preamplifier in the groups and are not arranged in openings in a passivation layer. Rather, Appellant contends different signals in Kawahara are distributed to the groups (App.

Br. 13; Reply Br. 16). In addition, Appellant argues that both Smith and Kawahara constitute non-analogous art (App. Br. 14; Reply Br. 17-18).

The Examiner notes that Kawahara teaches providing external power VE independently of other external connections -- a potential provided to at least two groups (circuits) (Ans. 18).

We will not sustain the Examiner's rejection of independent claims 27 and 40 essentially for the reasons indicated by Appellant. As we indicated previously, we find the secondary reference to Smith non-analogous art and cannot sustain the Examiner's rejection on that ground alone. Furthermore, even if we consider Kawahara's semiconductor IC device with sense amplifier relied upon by the Examiner (Kawahara, Fig. 17; col. 12, l. 66 - col. 14, l. 28) analogous art, the signals YR1, YW1, F21, F11 referred to by the Examiner on Page 8 of the Answer are all different signals that, in our view, are not equivalent to the recited potential -- a potential that must be independently distributed to all of the groups and at least one preamplifier in the groups as claimed.

Kawahara does indicate that VE is an external power source voltage (Kawahara, col. 14, ll. 62-63; Fig. 17a). But even assuming that this external voltage is distributed to multiple circuits as the Examiner indicates (Ans. 18), we still fail to see how the combined teachings of Kawahara and Smith teach or would have suggested the recited structural aspects of the claims, namely, with respect to the external connections being arranged in openings in a passivation layer adjacent to one or more interconnecting layers as claimed. Even if Smith were analogous art (which it is not), we still see no reasonable teaching or suggestion to pick and choose various aspects of the Smith reference (e.g., the transmit and receive element

connections routed through the multilayer ceramic (MLC) connector 850) and apply these unrelated teachings to Kawahara to ostensibly arrive at the claimed invention.

For at least the foregoing reasons, we will not sustain the Examiner's rejection of independent claims 27 and 40 or dependent claims 28-39 and 41-52 for similar reasons.[9]

DECISION

We have sustained the Examiner's rejections with respect to claims 1-26. We have not, however, sustained the Examiner's rejection with respect to claims 27-52. Therefore, the Examiner's decision rejecting claims 1-52 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

[9] Although we reverse the Examiner's rejection based on Kawahara and Smith, the Examiner may wish to consider the potential applicability of the admitted prior art in the Specification in conjunction with other prior art as it pertains to the patentability of claims 27-52. We leave this determination to the Examiner.

AFFIRMED-IN-PART

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HARNESS, DICKEY & PIERCE P.L.C.
5445 CORPORATE DRIVE
SUITE 200
TROY MI 48098