

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MATTHIAS EBERLEIN

Appeal 2008-0064
Application 10/347,983¹
Technology Center 2800

Decided: 21 March 2008

Before JAMESON LEE, RICHARD TORCZON and SALLY C. MEDLEY,
Administrative Patent Judges.

MEDLEY, *Administrative Patent Judge.*

DECISION ON APPEAL

¹ Application for patent filed 21 Jan. 2003. The real party in interest is Dialog Semiconductor GmbH.

A. Statement of the Case

This is an appeal under 35 U.S.C. § 134 from the Examiner's Final Rejection of claims 1 and 12². We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Spalding	US 6,663,198	Oct. 14, 2003
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Claims 1 and 12 stand rejected under 35 U.S.C. § 103(a) as unpatentable over the admitted prior art in view of Spalding.

BACKGROUND

The invention is related to a circuit and method for a low dropout (LDO) voltage regulator for overcoming performance degradation while the LDO is operating in the dropout region. The LDO circuit has a PMOS (p-channel Metal Oxide Semiconductor Field Effect Transistor) current mirror comprising transistors **31** and **32**, a supply voltage V_{DD} **34**, an output voltage **33**, a voltage divider comprising resistors **36** and **37** and an amplifier **35**. A regulated cascode structure comprising a transistor **41** and an error amplifier **42** is placed at the input of the PMOS current mirror to avoid performance degradation while operating in the low dropout region. (Abs., Spec. 2, 6-7 and 9 and **fig. 4**).

² Claims 3 and 8 were cancelled in the Response filed 05 May 2004, claims 4-7, 9-11 and 14-20 were cancelled in the Response filed 09 Aug. 2004 and claims 2 and 13 were cancelled in the response filed 20 Sept. 2004.

B. Issues

The issue before us is whether Applicant has shown that the Examiner erred in determining that claims 1 and 12 are unpatentable under 35 U.S.C. § 103(a) over the admitted prior art in view of Spalding?

For the reasons that follow, Applicant has failed to sufficiently show that the Examiner erred in determining that claims 1 and 12 are unpatentable under 35 U.S.C. § 103(a) over the admitted prior art in view of Spalding.

C. Findings of Fact (“FF”)

The record supports the following finding of facts as well as any other findings of fact set forth in this opinion by at least a preponderance of the evidence.

1. Applicant’s claims 1 and 12 are the subject of this appeal.
2. Claims 1 and 12 are independent claims.
3. Claims 1 and 12 stand or fall together (Br. 7).
4. Claims 1 is representative and is as follows:

A circuit to achieve a low drop-out (LDO) voltage regulator having a high performance in all operating conditions including the dropout region comprising:

a first amplifier having an inverting input, a non[-] inverting input, and an output wherein the non-inverting input is connected to a reference voltage;

a first transistor having gate connected to the output of said first amplifier;

a voltage divider comprising a string of two resistors; and

a current mirror having an input and an output wherein the input is connected the drain of said transistor and the output is connected to said voltage divider at the voltage regulated output, wherein the current mirror further comprises:

a second amplifier having an inverting input, a non-inverting input, and an output wherein said non-inverting input is connected to said voltage regulator output;

- a second transistor having source connected to the first transistor drain, gate connected to the second amplifier output, and drain connected to the second amplifier inverting input;
- a third transistor having source connected to the drain of the second transistor; and
- a fourth transistor having source connected to the regulated output and gate connected to both the gate of the third transistor and the source of the second transistor wherein said second, third, and fourth transistors are PMOS transistors.
5. The Examiner found that Applicant's admitted prior art figure 3 describes a circuit including an first amplifier **35** having an inverting input, a non-inverting input, and an output wherein the non-inverting input is connected to a reference voltage V_{ref} ; a first transistor having gate connected to the output of the first amplifier; a voltage divider comprising a string of two resistors **36, 37**; and a current mirror having an input and an output, wherein the input is connected to the drain of the transistor and the output is connected to the voltage divider at the voltage regulated output, wherein the current mirror further comprises a third transistor **31** and a fourth transistor **32** (Final Rejection 2 and Ans. 3 and Spec. **fig. 3**).
 6. The Examiner found that Applicant's admitted prior art figure 3 does not describe a regulated cascode structure having a first amplifier and a second transistor connected between the first transistor and the third transistor (Final Rejection 2 and Ans. 3).
 7. The Examiner found that Spalding describes a pull down current mirror circuit having a current mirror **MN1, MN2** and a regulated cascode structure **602, 407** coupled between the input and output of the current mirror and regulating the entry voltage of the current

- mirror to be equal to the output of the current mirror circuit (Final Rejection 2-3 and Ans. 3 and Spalding **fig. 7**).
8. The Examiner found that Spalding's current mirror circuit is capable of operating in a low headroom environment (Final Rejection 3 and Ans. 3-4).
 9. The Examiner concluded that it would have been obvious to one having ordinary skill in the art to add a regulated cascode structure as described by Spalding to the circuit described in Applicant's prior art figure 3 for the purpose of enabling the circuit to operate in a low headroom environment (Final Rejection 3 and Ans. 4).
 10. The Examiner also found that it is well known in the art that in order to convert a pull down current mirror circuit to a pull up current mirror circuit, the polarity or type of transistors in the current mirror circuit must be reversed (Final Rejection 3 and Ans. 4).
 11. The Examiner also found that Spalding describes in figure 10 a pull up current mirror circuit with PNP transistors and describes at column 6, lines 26-45 that FETs (field effect transistors) have equivalent function to bipolar transistors (Final Rejection 3 and Ans. 4).
 12. The Examiner found that the added cascode structure of Spalding must comprise p-channel transistors because Applicant's admitted prior art current mirror is a pull-up current mirror made of p-channel transistors.
 13. Applicant's Specification indicates that one of ordinary skill in the art would understand and appreciate that other types of transistors can be used for the current mirror such as NMOS, bipolar PNP transistors and bipolar NPN transistors if a regulator with a negative output voltage is constructed (Spec. 10).

D. Principles of Law

"[T]he law does not require that the references be combined for the reasons contemplated by the inventor." *In re Beattie*, 974 F.2d, 1309, 1312 (Fed. Cir. 1992).

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1734 (2007).

"Under §103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background the obviousness or nonobviousness of the subject matter is determined." *Id.*

In an obviousness analysis, it is not necessary to find precise teachings in the prior art directed to the specific subject matter claimed because inferences and creative steps that a person of ordinary skill in the art would employ can be taken into account. *Id.* at 1741.

E. Analysis

Independent claims 1 and 12 stand or fall together. We focus our analysis with respect to Claim 1. The Examiner found that Applicant's admitted prior art figure 3 describes the claimed invention with the exception of a regulated cascode structure having a first amplifier and a second transistor connected between the first transistor and the third

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transistor (FF³s 5-6). The Examiner found that Spalding describes a pull down current mirror circuit having a current mirror **MN1**, **MN2** and a regulated cascode structure **602**, **407** coupled between the input and output of the current mirror and regulating the entry voltage of the current mirror to be equal to the output of the current mirror circuit (FF 7). The Examiner concluded that it would have been obvious to one with ordinary skill in the art to add a regulated cascode structure as described by Spalding to the circuit described in Applicant's admitted prior art figure 3 for the purpose of enabling the circuit to operate in a low headroom environment since Spalding's current mirror circuit is capable of operating in a low headroom environment (FFs 8-9). The Examiner also found that it is well known in the art that in order to convert a pull down current mirror circuit to a pull up current mirror circuit, the polarity or type of transistors in the current mirror circuit must be reversed (FF 10). The Examiner also found that Spalding describes in figure 10 a pull up current mirror circuit with PNP transistors and describes at column 6, lines 26-45 that FETs (field effect transistors) have equivalent function to bipolar transistors (FF 11). As a result, the Examiner found that the added cascode structure of Spalding must comprise p-channel transistors because the admitted prior art current mirror is a pull-up current mirror made of p-channel transistors (FF 12).

Claim 1 recites "wherein said second, third, and fourth transistors are PMOS transistors". Applicant argues that neither Spalding nor Applicant's admitted prior art teach or suggest forming a regulated cascode structure using PMOS devices (p-channel Metal Oxide Semiconductor Field Effect Transistors) (Br. 7). Applicant argues that Spalding only shows a current

³ FF denotes Finding of Fact.

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mirror structure comprising NMOS devices (n-channel Metal Oxide Semiconductor Field Effect Transistors) or bipolar PNP devices and does not mention any role for PMOS devices in the invention (Br. 8).

Applicant's arguments do not rise to the level of showing error on the part of the Examiner. Applicant has not addressed the Examiner's findings with respect to the interchangeability of PMOS and NMOS transistors depending upon whether the current mirror is a pull-up current mirror or pull-down current mirror (FFs 10-12). Moreover, Applicant's Specification indicates that one of ordinary skill in the art would readily appreciate that other types of transistors can be used for the current mirror such as NMOS, bipolar PNP transistors and bipolar NPN transistors if a regulator with a negative output voltage is constructed (FF 13). For all of these reasons, Applicant's argument regarding the exchangeability of PMOS transistors is not persuasive.

Claim 1 also recites the limitation "a voltage divider comprising a string of two resistors". The Examiner found that Applicant's admitted prior art figure 3 describes a voltage divider comprising a string of two resistors **36**, **37** (FF 5).

Applicant argues that Spalding does not show a feedback mechanism using a string of resistors, but Applicant acknowledges that the admitted prior art describes a string of resistors (Br. 8). Applicant argues that there is no motivation to be found in Spalding or the admitted prior art to combine the teaching of a string of resistors for the purpose of creating the claimed invention (Br. 8). "[T]he law does not require that the references be combined for the reasons contemplated by the inventor." *In re Beattie*, 974 F.2d, 1309, 1312 (Fed. Cir. 1992). Moreover, the Examiner did not reason that it would have been obvious to one with ordinary skill in the art to add

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the voltage regulator including a string of resistors to the device of Spalding. Instead, the Examiner concluded that it would have been obvious to one with ordinary skill in the art to add a regulated cascode structure as described by Spalding to the circuit described in Applicant's prior art figure 3 for the purpose of enabling the circuit to operate in a low headroom environment (FF 9). Applicant did not address the Examiner's conclusion for combining Spalding with the prior art.

Applicant also argues that there is no motivation for combining the teachings of Applicant's admitted prior art with Spalding since Spalding does not teach or suggest applying the current mirror to a voltage regulator or any relationship between the output I_{out} and input I_{in} (Br. 9). In an obviousness analysis, it is not necessary to find precise teachings in the prior art directed to the specific subject matter claimed because inferences and creative steps that a person of ordinary skill in the art would employ can be taken into account. *KSR International Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1741 (2007).

Applicant has not addressed the Examiner's specific reasoning that the motivation to combine the references was for the purpose of enabling the circuit to operate in a low headroom environment (FF 9). Furthermore, Applicant appears to be attacking the Spalding reference alone, rather than the combination of Applicant's admitted prior art and Spalding. "Non-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references." *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986).

The prior art figure 3 describes that it was already known that a current mirror may be applied to a voltage regulator. The Examiner relied on Spalding for the teaching of a cascode circuit as it may be further applied to

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the prior art arrangement, e.g., the current mirror/voltage regulator, for the purpose of operating the prior art voltage regulator in a low headroom environment, thereby saving power consumption (Ans. 6).

For all these reasons we find that Applicant has failed to sufficiently show that the Examiner erred in determining that claims 1 and 12 are unpatentable under 35 U.S.C. § 103(a) over admitted prior art in view of Spalding.

F. Decision

Upon consideration of the record, and for the reasons given, the Examiner's rejections of claims 1 and 12 as unpatentable over Applicant's admitted prior art in view of Spalding are affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

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