

UNITED STATES PATENT AND TRADEMARK OFFICE

---

BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

---

*Ex parte* ZEYNEP M. TOROS, ESIN TERZIOGLU, and GIL WINOGRAD

---

Appeal 2008-0078  
Application 10/269,201  
Technology Center 2100

---

Decided: May 30, 2008

---

Before JAMES D. THOMAS, JEAN R. HOMERE,  
and ST. JOHN COURTENAY III, *Administrative Patent Judges*.

COURTENAY, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-28. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

## THE INVENTION

The disclosed invention relates generally to the field of testing embedded devices. More specifically, certain embodiments relate to a software programmable verification tool having a built-in self-test (BIST) for testing and debugging multiple memory modules in an embedded device under test (Spec. 1).

Independent claim 1 is illustrative:

1. A method for testing and debugging an embedded device under test, the method comprising:

loading an instruction into a parameterized shift register of a BIST module coupled to each one of a plurality of embedded memory modules comprising the device under test;

determining an identity of the loaded instruction; and

generating a plurality of test signals corresponding to said determined identity of said loaded instruction, each of said generated plurality of test signals causing control and execution of the testing and debugging of a corresponding one of each of said plurality of embedded memory modules comprising the embedded device under test.

## THE REFERENCE

The Examiner relies upon the following reference as evidence in support of the rejection:

Edwards

US 6, 665,816 B1

Dec. 16, 2003

### THE REJECTION

Claims 1-28 stand rejected under 35 U.S.C. §102(e) as being anticipated by Edwards.

### PRINCIPLES OF LAW

Appellant has the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006).

In rejecting claims under 35 U.S.C. § 102, “[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation.” *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005) (citation omitted). “Anticipation of a patent claim requires a finding that the claim at issue ‘reads on’ a prior art reference.” *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) (“In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art”) (internal citations omitted).

### Claim Construction

During prosecution, “the PTO gives claims their ‘broadest reasonable interpretation.’” *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). Here, we broadly but reasonable construe the claim term “BIST module” (built in self test circuit)

to encompass a test paradigm that incorporates circuitry in the device for executing and resolving test information about the device.

### Grouping of Claims

Appellants have argued the anticipation rejection of Edwards as ten groups that we address separately *infra* (see App. Br. 5-20). We select each of claims 1-9, and 28 as the representative claim for each group. See 37 C.F.R. § 41.37(c)(1)(vii)(2006).

After considering the record before us, it is our view that Edwards discloses each limitation argued by Appellants, as detailed in our analysis below.

### ANALYSIS

#### Claims 1, 10, and 19

Regarding representative claim 1, we find Edwards discloses loading an instruction into a parameterized shift register of a BIST module, as follows: Edwards teaches that the Test Data Input (TDI) is loaded into the shift register 1006 (Fig. 10). Fig. 10 shows that the instructions are decoded from the test input data by the instructions decode circuit 1005. Fig. 10 further illustrates that the shift register 1006 and instruction decode 1005 are part of the instruction register 1002. Thus, we find that Edwards discloses loading an instruction into a parameterized shift register. We further note that Edwards discloses that the instruction register is a part of the boundary scan circuit. The boundary scan circuit allows debug operations to be performed on an integrated circuit (col. 22 ll. 46-50).

We further note that Fig. 1 of Edwards illustrates a debug circuit 103 that is embedded in integrated circuit (SOC) 101 (col. 6 ll. 43-46). As discussed *supra*, we construe a BIST to encompass a test paradigm that incorporates circuitry in the device for executing and resolving test information about the device. Such is the case with the debug circuit 103 of Edwards (see for example col. 2 ll. 46-50). Thus, we find that Figs. 2 and 10 of Edwards teach a debug circuit and circuitry that executes and resolves test information about the integrated circuit, i.e., a BIST module.

We further find that Edwards teaches that the processor 102 contained in SOC 101, may read data from, or write data to a number of data stores that are accessible directly on the system bus 105 (see col. 6 ll. 56-64). Further, the element of embedded memory is prior art as admitted by Appellants (see Spec. 2, para. [0001]). Thus, Edwards teaches that the debug circuit 103 is coupled to a plurality of data stores via the processor 102. We further note that the teachings of Edwards do not preclude a finding that the data stores are internal to SOC 101 (col. 6 lines 56-64). Thus, we find that Edwards teaches a BIST module (Debug Circuit) coupled to a plurality of memory modules (i.e., data stores).

We further find that Fig. 10 of Edwards teaches the element of determining an identity of the loaded instruction. More specifically, as discussed *supra*, Edwards teaches an instruction decode register 1005 that is contained within an instruction register 1002. We conclude that an instruction that is decoded is also identified because the identity of the instruction would be obtained once the instruction is decoded.

We further find that Edwards teaches generating a plurality of test signals corresponding to the determined identity of the loaded instruction.

Appeal 2008-0078  
Application 10/269,201

We note that Appellants did not argue that Edwards fails to teach the element of the generated plurality of test signals causing control and execution of the testing and debugging of a corresponding one of each of the plurality of embedded memory modules, as recited in claim 1. We note that arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii)(2006). *See also In re Watts*, 354 F.3d 1362, 1368 (Fed. Cir. 2004).

In addition, as noted by the Examiner, the current claims do not specify where the test signals are generated. Appellants contend that this element is supported in the Specification (Reply Br. 8). However, while claims are interpreted in light of the specification, limitations cannot be read into the claims. *Superguide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004).

Thus, we find that Edwards teaches generating a plurality of test signals for the following reason: We agree with the Examiner's findings that Fig. 10 of Edwards teaches the instruction register 1002 supplies the address that allows one of the design-specific data registers 1009 to be accessed during a data register scan operation, i.e., generating test signals that correspond to the determined identity of the loaded instruction (col. 23 ll. 51-59).

Appellants further contend that Edwards discloses an Integrated Circuit that communicates with an external system (App. Br. 7-8). Moreover, according to Appellants, Edwards teaches that the generated signals originate from an external system 106 which is not a part of the

claimed BIST (see App. Br. 7 § C). We conclude that this assertion is irrelevant for the following reasons:

Firstly, as discussed above, the current claims do not limit the origin of the generated signals. Thus, this element can broadly but reasonably be interpreted to comport with the Examiner's findings that the external signals may be generated externally, i.e., the external system 106 of Edwards (see Ans. 8, ll. 6-12).

Secondly, as discussed *supra*, we find that Edwards teaches generating the plurality of signals from within the debug circuit shown in Figs. 2 and 10. Thus, for the reasons discussed *supra*, we find Appellants' contentions regarding the external system of Edwards to be unpersuasive.

Appellants further contend that the JTAG processor 207 of Edwards is not a BIST module (App. Br. 8 § D). As discussed *supra*, we find that at least Figs. 1, 2, and 10 of Edwards teach a debug circuit 103 and/or circuitry that executes and resolves test information about the integrated circuit 101. Appellants contend that the JTAG processor is controlled by the external system 106 and therefore is not part of a BIST module. We do not find this argument to be persuasive. Even if *arguendo* the external system 106 supplies the instructions and generated test signals, the current claims do not state the origin of either the instructions or the generated signals. Thus, a broad but reasonable interpretation of claim 1 allows for the data and/or signals to be generated externally.

Appellants further contend that the debug circuit of Edwards is not a BIST module. More specifically, Appellants contend that debugging is not the same as testing the integrity of the chip (App. Br. 9 § E). We find that Appellants' own arguments contradict this assertion. Appellants reference a

Appeal 2008-0078  
Application 10/269,201

definition of “debug” which states “[t]o examine or test . . .” (emphasis in original) (Reply Br. 10). Thus, while debugging and testing may not necessarily go hand in hand, the citation to a debugging circuit does not preclude a finding that the debug circuit of Edwards also performs testing. Moreover, Appellants’ Specification states that boundary scan techniques (such as those described in Fig. 10 of Edwards at col. 10 ll. 46-50) are used to “facilitate tasks such as testing debugging and verification” (Spec. 2, para [0001]). Still further, as discussed *supra*, Figs. 2 and 10 of Edwards perform the recited functions of the claimed BIST module. Thus, at least for these reasons, we are not persuaded by Appellants’ contention that the debug circuit of Edwards is not a BIST module.

Therefore, for at least the reasons stated above, we conclude that Appellants have not shown the Examiner erred. Accordingly, we sustain the Examiner’s rejection of independent claim 1 (and independent claims 10 and 19 that fall therewith) as being anticipated by Edwards.

#### Claims 2, 11, and 20

Regarding representative claim 2, Appellants contend that Edwards fails to teach distributing each of the generated plurality of test signals sequentially to said a corresponding one of each of said plurality of embedded memory modules comprising the embedded device under test, as claimed (App. Br. 12-13). Appellants then merely restate what Edwards discloses, and reassert that Edwards does not disclose the aforementioned claim limitations (App. Br. 12-13). Thus, Appellants have made a general allegation in the Brief that the representative claim defines a patentable

Appeal 2008-0078  
Application 10/269,201

invention without specifically pointing out how the language of the claim patentably distinguishes over the cited Edwards reference. A statement which merely points out what a claim recites will not be considered an argument for separate patentability of the claim. *See* 37 C.F.R. § 41.37(c)(1)(vii). The Examiner, as finder of fact, has determined that the debug circuit provides a number of state values to processor 102 for use in debugging operations, and therefore, meets the argued limitations (*see* Ans. 12). It is our view that Appellants have failed to rebut the Examiner's rejection with respect to these limitations with any meaningful analysis that explains why the Examiner erred. On this record, we conclude that Appellants have failed to meet their burden of showing error in the Examiner's prima facie case of anticipation for representative claim 2 (and claims 11 and 20 that fall therewith). Accordingly, we sustain the Examiner's rejections of claims 2, 11, and 20 as being anticipated by Edwards.

#### Claims 3, 12, and 21

Regarding representative claim 3, Appellants contend that Edwards fails to teach "generating at least one clock signal from a host application software, and at least one clock signal controlling said loading of said instruction into said parameterized shift register," as claimed (App. Br. 13). More specifically, Appellants contend that clock signal TCK is provided by the external system 106 of Edwards, and not by the host application software as recited in claim 3 (App. Br. 13-14).

We agree with the Examiner's determination that Edwards teaches that the clock signal is provided by software stored on the external system 106 (see col. 7 ll. 39-41). Furthermore, Edwards teaches that the external system 106 performs the functions of a host processor, i.e., generating and providing system clock signals. In addition, Appellants acknowledge that a host is "well-known in the art" (see Reply Br. 12). Therefore, we conclude that Appellants have not shown the Examiner erred. Accordingly, we sustain the Examiner's rejection of representative claim 3 (and claims 12 and 21 that fall therewith) as being anticipated by Edwards.

#### Claims 4, 13, and 22

Regarding representative claim 4, Appellants contend that Edwards fails to teach "shifting said instruction into said parameterized shift register of said BIST module," as claimed (App. Br. 13-14). At least for the reasons discussed *supra* regarding claim 1, we find that Fig. 10 of Edwards teaches these limitations (see Fig. 10, refs. 1002, 1005 and 1006). Therefore, we conclude that Appellants have not shown the Examiner erred. Accordingly, we sustain the Examiner's rejection of representative claim 4 (and claims 13 and 22 that fall therewith) as being anticipated by Edwards.

#### Claims 5, 14, and 23

Regarding representative claim 5, Appellants contend that Edwards fails to teach "identifying a command within said instruction shifted into said parameterized shift register," as claimed (App. Br. 15). Appellants then merely restate what Edwards discloses, and reassert that Edwards does not disclose the aforementioned claim limitations (App. Br. 15-16). Therefore,

Appeal 2008-0078  
Application 10/269,201

we conclude that Appellants have not met their burden of showing that the Examiner erred. Accordingly, we sustain the Examiner's rejection of representative claim 5 (and claims 14 and 23 that fall therewith) as being anticipated by Edwards.

#### Claims 6, 15, and 24

Regarding representative claim 6, Appellants contend that Edwards fails to teach "decoding said identified command," as claimed (App. Br. 16-17). In response to the Examiner's Answer, Appellants have failed to rebut the Examiner's new findings in any meaningful way. In particular, Appellants have failed to respond (in the Reply Brief) to the Examiner's new finding that "[t]he instruction decoder of Figure 10 decodes the identified command." (Ans. 14). In the Reply Brief, Appellants state that "it is unclear what the Examiner is referring to by citing Figure 10 of Edwards, since Edwards (including Figure 10) does not teach or suggest 'said identifying further comprises decoding said identified command,' as recited by the Appellants in claim 6." (Reply Br. 14). We note that "instruction decode 1005" is shown clearly in Figure 10 of Edwards. Because Appellants have not shown the Examiner erred, we sustain the Examiner's rejection of representative claim 6 (and claims 15 and 24 that fall therewith) as being anticipated by Edwards.

#### Claims 7, 16, and 25

Regarding representative claim 7, Appellants contend that Edwards fails to teach loading test results from said each one of a plurality of embedded memory modules . . . into said parameterized shift register of

Appeal 2008-0078  
Application 10/269,201

said BIST module, as claimed (App. Br. 17). Appellants again repeat the familiar pattern of (1) asserting that the reference does not disclose the claim language, followed by, (2) restating what the cited portion of Edwards discloses, and, (3) reasserting that Edwards does not disclose the claim limitations (*see* App. Br. 17). Appellants additional comments in the Reply Brief do not remedy the deficiency of the Appeal Brief (*see* Reply Br. 14). We conclude that Appellants have failed to rebut the Examiner's rejection with respect to these limitations with any meaningful analysis that explains why the Examiner erred. Because Appellants have not shown the Examiner erred, we sustain the Examiner's rejection of representative claim 7 (and claims 16 and 25 that fall therewith) as being anticipated by Edwards.

#### Claims 8, 17, and 26

See our discussion of claims 7, 16, and 25 above. Here again, Appellants merely give a recitation of claims, and a recitation of the Examiner's citation of Edwards, followed by the conclusion that the cited portion of Edwards does not disclose or suggest the limitations of representative claim 8 (App. Br. 18). On this record, we conclude that Appellants have failed to meet their burden of showing error in the Examiner's prima facie case of anticipation for representative claim 8 (and claims 17 and 26 that fall therewith). Accordingly, we sustain the Examiner's rejection of claims 8, 17, and 26 as being anticipated by Edwards.

Claims 9, 18, and 27

See our discussion of claims 8, 17, and 26 above. For the same reasons discussed above, we conclude that Appellants have failed to rebut the Examiner's rejection with any meaningful analysis that explains why the Examiner erred. In particular, in the Reply Brief, Appellants have failed to counter the Examiner's findings on page 15 of the Answer. Because Appellants have not shown the Examiner erred, we sustain the Examiner's rejection of representative claim 9 (and claims 18 and 27 that fall therewith) as being anticipated by Edwards.

Claim 28

See our discussion of claims 8, 17, and 26 above. For the same reasons discussed above, we conclude that Appellants have failed to rebut the Examiner's rejection with any meaningful analysis that explains why the Examiner erred. In particular, in the Reply Brief Appellants have failed to counter the Examiner's findings on page 16 of the Answer. Because Appellants have not shown the Examiner erred, we sustain the Examiner's rejection of claim 28 as being anticipated by Edwards.

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that Appellants have not met their burden of showing that the Examiner erred in rejecting claims 1-28 under 35 U.S.C. § 102(e) for anticipation.

Appeal 2008-0078  
Application 10/269,201

DECISION

We affirm the Examiner's decision rejecting claims 1-28.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

pgc

MCANDREWS HELD & MALLOY, LTD  
500 WEST MADISON STREET  
SUITE 3400  
CHICAGO IL 60661