

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte ERIC J. CRABILL*

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Appeal 2008-0129  
Application 10/417,775  
Technology Center 2100

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Decided: September 16, 2008

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Before HOWARD B. BLANKENSHIP, JEAN R. HOMERE, and  
JAY P. LUCAS, *Administrative Patent Judges*.

BLANKENSHIP, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1-32, which are all the claims in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Claim 1 is illustrative.

1. A method of using a dedicated processor embedded in a Programmable Logic Device (PLD) to emulate a target processor, the dedicated processor supporting a first instruction set and conforming to a first bus protocol, the target processor supporting a target instruction set and conforming to a target bus protocol, the method comprising:

configuring first programmable resource of the PLD to implement a first bus interface unit, the first bus interface unit having a first port coupled to the dedicated processor and conforming to the first bus protocol, and further having a second port conforming to the target bus protocol; and

executing in the dedicated processor an emulation program that emulates the target instruction set while executing instructions from the first instruction set, the emulation program interacting with the first bus interface unit via the first port,

wherein the target instruction set is different from the first instruction set, and

wherein the target buts protocol is different from the first bus protocol.

The Examiner relies on the following reference as evidence of unpatentability.

Taylor                    US 5,535,342                    Jul. 9, 1996

Claims 1-32 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Taylor.

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984). “[A]bsence from the reference of any claimed element negates anticipation.” *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565, 1571 (Fed. Cir. 1986).

We do not sustain the rejection of claims 1-32 substantially for the reasons expressed by Appellant in the briefs. The rejection fails to set forth a *prima facie* case for anticipation over Taylor.

The statement of rejection points to different elements of Taylor that are deemed to correspond to some of the terms recited in the claims. However, the rejection does not account for all the limitations as they are set out, and interrelated, in the claims.

Claim 1, for example, recites a method of using a dedicated processor embedded in a PLD (Programmable Logic Device) to emulate a target processor, for which the rejection refers to column 7, lines 33 through 35 of Taylor. (Ans. 3.) Taylor at column 7, lines 33 through 42, describes a PLD. Where does the section describe a dedicated processor embedded in the PLD? Where does the section describe a target processor to be emulated?

The statement of rejection goes on to assert that column 28, lines 44 through 49 of Taylor describes the unspecified “dedicated processor” supporting a first instruction set and conforming to a first bus protocol. (Ans. 3.) The indicated section of Taylor describes a “first bus interface” that must be deemed to be the “first bus protocol.” Where does the section describe a first instruction set?

Similar problems occur with the mapping to Taylor of the claimed target instruction set, target bus protocol, and first bus interface unit having a first port coupled to the “dedicated processor” and conforming to the “first protocol,” further having a second port conforming to the “target bus protocol.”

The rejection of claim 1 also appears to contend that Taylor at column 23, lines 27 through 40 (Ans. 4), or perhaps column 25, lines 45 through 62 (Ans. 16), or maybe column 25, lines 58 through 59 (*id.*), or maybe column 21, line 54 through column 22, line 6 (*id.*), or maybe column 23, line 62 through column 24, line 3 (Ans. 16-17), discloses some kind of “emulation,” which we can assume to be true. However, we are left to speculate how “executing in the dedicated processor an emulation program that emulates the target instruction set while executing instructions from the first instruction set” might be deemed to be met by the reference disclosure, because we are left to speculate what might be deemed the “dedicated processor,” the “emulation program,” the “target instruction set,” and the “first instruction set.”

The rejection applied against at least the remainder of the independent claims (9, 17, and 25) suffers from similar deficiencies. We thus cannot sustain the rejection of any claim on appeal.

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## CONCLUSION

The rejection of claims 1-32 under 35 U.S.C. § 102(b) as being anticipated by Taylor is reversed.

REVERSED

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