

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAREL N. EMMOT and ERIC M. RENTSCHLER

Appeal 2008-0143
Application 10/154,649
Technology Center 2100

Decided: September 9, 2008

Before HOWARD B. BLANKENSHIP, ALLEN R. MACDONALD, and
CAROLYN D. THOMAS, *Administrative Patent Judges*.

BLANKENSHIP, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1-12. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

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Appellants' invention relates to a fully mirrored mirror system that includes a split memory bus, where each portion of the split memory bus has an active memory and a mirror memory. (Abstract.) Claim 1 is illustrative.

1. A computer system, comprising:

- a memory controller controlling a memory bus, the memory bus split into a plurality of portions, where in response to a memory transaction each portion of the memory bus transfers a portion of the data; and
- a plurality of memory units coupled to each portion of the memory bus, each memory unit having a corresponding mirror memory unit on the same portion of the memory bus.

The Examiner relies on the following reference as evidence of unpatentability.

MacLaren US 6,785,835 B2 Aug. 31, 2004

Claims 1, 3, 6, and 7 stand rejected under 35 U.S.C. § 102(e) as being anticipated by MacLaren.

Claims 2, 4, 5, and 8-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over MacLaren.

Claims 13-15 have been allowed.

Section 102 rejection over MacLaren

Based on Appellants' arguments in the Appeal Brief, we will decide the appeal of the § 102(e) rejection on the basis of claims 1 and 3. *See* 37 C.F.R. § 41.37(c)(1)(vii).

The Examiner reads instant claim 1 on MacLaren in findings set forth at page 4 of the Answer. Appellants argue that claim 1 specifies a memory controller controlling a memory bus, and allege that MacLaren describes neither.

Claim 1 does specify a memory controller controlling a memory bus. However, the claim's only requirement of the memory controller is that it controls "a memory bus." The Examiner reads the "memory bus" on individual bus segments 22A through 22E (bus 22) (Fig. 1) of MacLaren, over which data controller 18, in association with host controller 16, transmits data. MacLaren col. 6, ll. 31-44. Host/data controller 16, 18 controls the bus at least during transfer of data to the five memory controllers 20A through 20E. MacLaren thus supports the Examiner's finding that MacLaren describes a "memory controller" as claimed.

As Appellants note, MacLaren describes host/data controller 16, 18 (Fig. 1) as being coupled to memory controllers 20. MacLaren col. 5, ll. 42-59. Claim 1, however, is not limited to a "computer system" having a single "memory controller." Further, Appellants have produced no evidence tending to show that the artisan would never consider the data controller 18 in the reference, in view of the associated claim requirements and the broadest reasonable interpretation of the relevant term, as a type of "memory controller" within the meaning of claim 1. That MacLaren does not refer to structure 18 using the same words when denoting "memory controllers" 20 is *some* evidence but, without more, not persuasive evidence of some limiting definition known to the artisan that would serve to distinguish over the prior art. For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a

single reference. However, this is not an “ipsissimis verbis” test. *In re Bond*, 910 F.2d 831, 832 (Fed. Cir. 1990).

Appellants’ argument thus reduces to whether bus segments 22A through 22E are properly considered to constitute a “memory bus.”

Appellants allege that MacLaren column 5, lines 49 through 51 and column 6, line 47 describe bus 22 as “a data bus, not a memory bus,” (App. Br. 5), but we are unable to find such a description in the indicated passages. Appellants also draw our attention to column 26, lines 37 through 55 of the reference, submitting that “data” bus 22 “is used to decouple the host and data controllers from interfacing directly to the memory segments 24.” (App. Br. 5.) However, the quoted portion of MacLaren does not refer to a “data” bus 22. Moreover, had Appellants continued one line past the submitted quote from MacLaren, Appellants would have reproduced words that somewhat weaken the position that MacLaren does not describe a memory bus: “The MNET bus 22 is a point-to-point, general-purpose MEMORY BUS.” MacLaren col. 26, ll. 45-46 (emphasis added).

We thus are not persuaded of any error in the Examiner’s finding that MacLaren anticipates claim 1. We sustain the rejection of claim 1, and that of claims 6 and 7 which fall with claim 1.

In support of claim 3, Appellants submit that in MacLaren chip-select signals are generated by decode logic 62 (Fig. 3) in memory controller 20. (App. Br. 6.) *See also* MacLaren col. 8, ll. 40-53. As such, according to Appellants, there is no “necessary requirement” for data controller 18 to have any knowledge or control of which memory units are selected by the memory controllers 20. Appellants again refer to column 26, lines 37 through 55 of MacLaren, submitting that “data bus 22” [sic; memory bus 22]

is used to decouple the host and data controllers from interfacing “directly” to the memory segments 24. (App. Br. 6.)

Appellants’ arguments are not commensurate with the actual scope of instant claim 3. The claim does not require any kind of direct or continuous connection between the memory controller and a memory unit. The claim defines the “select-signal control lines” by the function “where” the lines “select a memory unit and its corresponding mirror memory unit to respond to a memory write transaction.” We also observe that the claim does not require any kind of internal distinction between a memory unit and “its corresponding mirror memory unit.”

MacLaren teaches that bus interface 60 (Fig. 3) is provided to meet the protocol and timing requirements of the MNET bus 22 for receiving write data and commands, and for transmitting read data and status. MacLaren col. 8, ll. 36-39. We agree with the Examiner that a form of “select-signal control lines,” as functionally defined in claim 3, are necessarily present between data controller 18 (MacLaren Fig. 1) and bus interface 60 (Fig. 3) in memory controller 20. If this were not so, the bus interface would not be apprised of valid data being present on MNET bus 22. Further, as Appellants acknowledge, decode logic 62 of MacLaren (Fig. 3) decodes the destination of memory (e.g., write) transactions according to commands from bus 22, and generates chip-select signals. MacLaren col. 8, ll. 40-45. At least the combination of lines between data controller 18 and the destination memory units falls within the meaning of the “select-signal control lines” as broadly claimed.

We are therefore not persuaded of error in the Examiner’s finding of anticipation with respect to claim 3. We sustain the rejection of claim 3.

Section 103 rejection over MacLaren

Appellants submit (twice) that “[c]laims 9, 10, and 12 specify select-signal control lines from the memory controller to the memory units.” (App. Br. 7.) We disagree. None of claims 9, 10, and 12 are so limited.

We will decide the appeal of the § 103(a) rejection on the basis of claim 9.¹ *See* 37 C.F.R. § 47.37(c)(1)(vii).

Claim 9 recites the step of “using select-signal control lines to select the first and second memory units for writing.” Appellants admit that memory controllers 20A through 20E “inherently have signal select lines for selecting memory units,” but argue that MacLaren does not teach or suggest that data controller 18 has signal-select lines from the memory controller to the memory units. Appellants further argue that the reference does not teach or suggest that data controller 18 selects memory units in response to a memory read or write transaction. (App. Br. 7.)

Claim 9 does not specify select-signal control lines from the memory controller to the memory units, and does not specify what may be “using” select-signal control lines. At least for the reason that the claim does not require the features argued to be missing from MacLaren, we are not persuaded of error in the rejection. We sustain the rejection of claim 9, and that of claims 2, 4, 5, 8, and 10 through 12 which fall with claim 9.

¹ Appellants place claim 8 in a separate heading in the Appeal Brief, but do not provide separate arguments in support of the claim. We have considered the arguments in nominal support of claim 8 in our review of the rejection of claim 1.

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CONCLUSION

The rejection of claims 1, 3, 6, and 7 under 35 U.S.C. § 102(e) as being anticipated by MacLaren is affirmed.

The rejection of claims 2, 4, 5, and 8-12 under 35 U.S.C. § 103(a) as being unpatentable over MacLaren is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

tdl/ce

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