

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MEHDI HATAMIAN

Appeal 2008-0221
Application 10/938,008
Technology Center 2100

Decided: July 28, 2008

Before ALLEN R. MACDONALD, JAY P. LUCAS,
ST. JOHN COURTENAY III, *Administrative Patent Judges*.

COURTENAY, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 90-94, 102-107, and 115-119. Claims 90-119 are pending. The Examiner has withdrawn the rejection under 35 U.S.C. § 102(b) of dependent claims 95 and 96 (Ans. 2). The Examiner has also withdrawn the rejection of claims 90-112 under 35 U.S.C. § 112, second

paragraph (*id.*). In the Final Office Action, the Examiner indicated that claims 97-101 and 108-114 would be allowable if rewritten in independent form pending resolution of the § 112, second paragraph issues (Final Action, 3). We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM IN PART.

THE INVENTION

The disclosed invention relates generally to area-efficient digital elements, such as digital filters. More particularly, Appellant's invention is directed to apparatus and methods for improving spatial efficiency and related performance in finite impulse response (FIR) filters in a high speed communication system (Spec. 1).

Independent claims 90 and 104 are illustrative:

90. A digital element, comprising:

an input data path having a first plurality of input bit locations arranged in a predetermined input bit-order sequence; and

a plurality of functional elements adapted to perform at least one preselected function,

wherein at least one of said plurality of functional elements is coupled to said input data path via a second plurality of input bit locations within said at least one of said plurality of functional elements, and

wherein said second plurality of input bit locations comprises a permuted bit-order sequence within said at least one of said plurality of functional elements, such that an interconnect comprising said input data path and disposed between said first plurality of input bit locations and said second plurality of input bit locations is rendered substantially direct and of minimized length.

104. A digital element, comprising:

an input data path;

an output data path;

a first component coupled to said input data path;

a second component coupled to said output data path;

at least one functional element being adapted to perform at least one preselected function and having a plurality of bit locations;

a first intermediate interconnect coupling said first component to said at least one functional element; and

a second intermediate interconnect coupling said second component to said at least one functional element,

wherein said at least one functional element is adapted to provide at least one of:

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a transposed permuted bit-order sequence and a permuted bit-order sequence on a selected portion of said plurality of bit locations coupled to said first intermediate interconnect and said second intermediate interconnect, such that an intermediate data path comprising said first intermediate interconnect and said second intermediate interconnect is rendered substantially direct and of minimized length.

THE REFERENCE

The Examiner relies upon the following reference as evidence in support of the anticipation rejection:

Ueda US 5,887,033 Mar. 23, 1999

THE REJECTION

Claims 90-94, 102-107, and 115-119 stand rejected under 35 U.S.C. §102(b) as being anticipated by Ueda.

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 102, “[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation.” *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005) (citation omitted).

“Anticipation of a patent claim requires a finding that the claim at issue ‘reads on’ a prior art reference.” *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) (“In other words, if granting patent protection on

the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.”) (internal citations omitted).

FINDINGS OF FACT

The following findings of fact (FF) are supported by at least a preponderance of the evidence:

1. Ueda discloses that bus state changes consume power, such as changing the state of one or more bits on a bus, due to load capacitance and other factors (col. 4, l. 63 through col. 5, l. 5).
2. Ueda discloses that power consumption may be reduced by manipulating the data bits on a bus in combination with a signal indicative of such manipulated state (e.g., instead of inverting all the bits for the next data word, merely sending a signal that indicates that the next bus data word should be inverted at the receiving end, thereby avoiding any bus state changes and associated power consumption (col. 5, ll. 5-19).
3. Ueda’s system is not limited to only bit inversion, but also encompasses transposition of bit order, compression/expansion, or a combination thereof, so long as the aggregate state change of the bus wiring (and associated

power consumption) is reduced by the manipulation (col. 5, ll. 19-24).

4. Ueda's system is directed to internal buses (i.e., a bus within an integrated circuit) as well as to external buses that connect integrated circuits (col. 5, ll. 25-34).
5. Ueda discloses a judgment section 10 (Fig. 3) that determines the relative magnitudes of manipulated and non-manipulated bus state changes, so as to determine whether or not such bit manipulation will result in lower power consumption (col. 5, ll. 37-54, col. 6, ll. 14-22).
6. Ueda discloses a Judgment section 10 (Fig. 3) that outputs a judgment signal 1507 which is supplied as a control input to Bit order transposing circuit 1508 (Figs. 17 and 20) (col. 16, l. 62 through col. 17, l. 1).
7. Ueda discloses that Bit order transposing circuit 1508 manipulates or transposes the bit order on the bus (col. 17, ll. 1-9, Figs. 17 and 20).

ANALYSIS

Independent Claim 90

We consider the Examiner's rejection of independent claim 90 as being anticipated by Ueda.

After reviewing the record before us, we address arguments presented in the Briefs only to the extent that Appellant's arguments are directed to claimed subject matter. Patentability is based upon the claims. "It is the *claims* that measure the invention." *SRI Int'l v. Matsushita Elec. Corp. of America*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (*en banc*). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989)).

Regarding independent claim 90, Appellant contends that:

Ueda does not disclose or suggest at least the limitation of "an input data path having *a first plurality of input bit locations* arranged in a predetermined input bit-order sequence . . . wherein at least one of said plurality of functional elements is coupled to said input data path via a second plurality of input bit locations . . . wherein *said second plurality of input bit locations comprises a permuted bit-order sequence* within said at least one of said plurality of functional elements," as claimed by the Applicant in independent claim 90.

(App. Br. 8, ¶ 1, emphasis in original).

Claim Construction

During prosecution, "the PTO gives claims their 'broadest reasonable interpretation.'" *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)).

We consider the scope of the argued claim term "permuted bit order." (Claim 90). Appellant defines the term "permuted bit order," as follows:

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As used herein, a "permuted bit-order" functional element, or digital element, includes any functional or digital element, as defined above, with a data path having a predetermined bit-order ordinal discontinuity.
(Spec. 9, ll. 10-13).

We note that the Examiner has read the “second plurality of input bit locations comprises a permuted bit-order sequence” on the angled input lines that connect each of input Bits 7-0 (i.e., the “first plurality of input bit locations arranged in a predetermined input bit-order sequence”) to the inputs of each of adjacent logic gate blocks 1801-1808 (i.e., functional elements as shown in the dotted rectangles of Ueda’s Figure 20). Ueda’s Figure 20 depicts the internal details of the Bit order transposing circuit 1508 shown in Figure 17.

For example, Bit 6 of logic gate block 1802 is provided as an input to one of the two AND gates of logic gate block 1801, as shown in Fig. 20. Likewise, Bit 7 of logic gate block 1801 is provided as an input to the uppermost AND gate of logic gate block 1802 (Ueda, Fig. 20). Therefore, we see no error with the Examiner’s reading of the “second plurality of input bit locations comprises a permuted bit-order sequence” on the AND gate inputs (i.e., second plurality) connected by the angled input lines to each of input Bits 7-0 (i.e., first plurality), because these angled input lines provide a data path having a predetermined bit-order ordinal discontinuity with respect to the adjacent logic gate blocks 1801-1808 (i.e., functional elements) (*see*

also FF 6 and 7). In describing Figure 20, Ueda expressly discloses transposing the bit order (col. 17, l. 3).

In the Reply Brief, Appellant presents a new argument that Ueda discloses a plurality of interconnects where there is *no single interconnect* between the first plurality of input bit locations and the second plurality of input bit locations (Reply Br. 5-6).¹ Appellant refers to five interconnects, with the second interconnect (shown as two angled connections between logic gate blocks pairs 1801 and 1802 in Ueda's Fig. 20) having the purpose of duplicating bits 7 and 6 (Reply Br. 6, ¶ 1). Because this "second interconnect," as described in Appellant's own words, is used "for purposes of duplicating [plural] bits 7 and 6," it is our view that this portion of Ueda fairly discloses "an interconnect comprising said input data path and disposed between said first plurality of input bits locations and said second plurality of input bit locations," as claimed (*see* Reply Br. 6, ¶1, line 4; *see also* claim 90).

For at least the aforementioned reasons, we find the weight of the evidence supports the Examiner's position. Because we conclude that

¹ We have discretion regarding whether we consider newly presented arguments filed after the opening brief. *See Optivus Tech., Inc. v. Ion Beam Applications S.A.*, 469 F.3d 978, 989 (Fed. Cir. 2006) (an issue not raised in an opening brief is waived). *But cf. Becton Dickinson and Co. v. C.R. Bard, Inc.*, 922 F.2d 792, 800 (Fed. Cir. 1990) ("This practice is, of course, not governed by a rigid rule but may as a matter of discretion not be adhered to

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Appellant has not shown the Examiner erred, we sustain the Examiner's rejection of independent claim 90 as being anticipated by Ueda.

Dependent claims 91-94, 102, and 103

We consider next the Examiner's rejection of dependent claims 91-94, 102, and 103 as being anticipated over Ueda. We note again that the Examiner has withdrawn the rejection under 35 U.S.C § 102(b) of dependent claims 95 and 96 (Ans. 2)

Although the Examiner rejected these claims under 35 U.S.C. § 102(b) in the Final Office action (*see* p. 2), the Examiner did not provide a detailed statement of rejection for each of these dependent claims until the Examiner's Answer (*see* Ans. 4). In spite of the absence of a more detailed statement of rejection for these dependent claims in the Final Office Action, we nevertheless note that it is Appellant who has the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006).

We have considered Appellant's response for each of dependent claims 91-94, 102, and 103, as separately argued in the Brief (*see* App. Br. 12-19). With respect to each of claims 91-94, 102, and 103, Appellant has: (1) merely recited the language of the claim, and (2) asserted that the limitations are not disclosed by Ueda (*id.*).

where circumstances indicate that it would result in basically unfair

Significantly, even though the Examiner provided a more detailed statement of rejection for each of dependent claims 91-94, 102, and 103 in the Answer (*see* Ans. 4), Appellant chose not to address the specifics of the Examiner's factual findings in the Reply Brief. Instead, Appellant merely states that "dependent claims 91-94 and 102-103 are allowable at least for the reasons stated above with regard to claim 90." (Reply Br. 9, ¶2).

In response, we see no deficiencies with the Examiner's rejection of claim 90, as discussed *supra*. Moreover, Appellant has failed to comply with the requirements of 37 C.F.R. § 1.111(b) by merely reciting the language of the claim and asserting that such language is not taught by the reference. We also note that a statement which merely points out what a claim recites will not be considered an argument for separate patentability of the claim. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Thus, Appellant has failed to show error in the Examiner's factual findings regarding dependent claims 91-94, 102, and 103 by explaining why the Examiner erred, even though Appellant had full opportunity to respond in the Reply Brief to the Examiner's more detailed findings, as set forth in the Answer (*see* Ans. 4). Accordingly, we sustain the Examiner's rejection of claims 91-94, 102, and 103 as being anticipated by Ueda.

procedure.") (citations omitted).

Independent Claim 104

We consider next the Examiner's rejection of independent claim 104 as being anticipated by Ueda.

Regarding independent claim 104, Appellant contends:

With regard to the rejection of independent claim 104 under Ueda, the Applicant submits that Ueda does not disclose or suggest at least the limitation of "wherein said at least one functional element is adapted to provide at least one of: a transposed permuted bit-order sequence and a permuted bit-order sequence on a selected portion of said plurality of bit locations coupled to said first intermediate interconnect **and** said second intermediate interconnect, such that an intermediate data path comprising said first intermediate interconnect **and** said second intermediate interconnect is rendered substantially direct and of minimized length," as claimed by the Applicant in independent claim 104 (emphasis added).

(App. Br. 9, ¶ 2).

We agree. We note that the Examiner has read the claimed "first intermediate interconnect" on the connection shown between output latch 103 and Bit order transposing circuit 1508 (*see* Ueda, Fig. 17). The Examiner has read the claimed "second intermediate interconnect" on the connection shown between Bit order transposing circuit 1508 and Terminal driving circuit 109 (Ueda, Fig. 17). Because the Examiner has read the claimed "at least one functional element" on Bit order transposing circuit 1508, we agree that Bit order transposing circuit 1508 only provides its transposed output to the (second) intermediate interconnect clearly shown as the connection between Bit order transposing circuit 1508 and Terminal

driving circuit 109 in Ueda's Figure 17. Therefore, Ueda's Bit order transposing circuit 1508 (i.e., "at least one functional element") does not provide a transposed bit-order sequence to *both* first *and* second intermediate interconnects in the manner claimed (Ueda, Fig. 17). We note that "absence from the reference of any claimed element negates anticipation." *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565, 1571 (Fed. Cir. 1986).

Because we conclude that Appellant has met his burden of showing that the Examiner has failed to establish a prima facie case of anticipation, we reverse the Examiner's rejection of independent claim 104 as being anticipated by Ueda. Since each associated dependent claim includes all the limitations of the claims from which it depends, we also reverse the Examiner's rejections of dependent claims 105-107 and 115-118 that depend directly or indirectly upon independent claim 104.

Independent Claim 119

Lastly, we consider the Examiner's rejection of independent claim 119 as being anticipated by Ueda.

Regarding independent claim 119, Appellant contends:

Applicant submits that Ueda does not disclose or suggest at least the limitation of "wherein said plurality of functional elements is operably disposed within the digital module, and at least one interconnect between at least a first functional element and at least a second functional element from said plurality of functional elements is rendered substantially direct and of

minimized length, based on said selective permuting," as claimed by the Applicant in independent claim 119. (App. Br. 10, ¶2).

We agree with the Examiner that a broad but reasonable construction of the language of the claim reads on Ueda's logic gate blocks 1801-1808 (Figure 20) (i.e., "providing a plurality of function elements having bit locations") where Bit order transposing circuit 1508 (shown in detail in Figure 20 and in block form in Figure 17) performs the claimed function of selectively permuting at least a portion of bit locations (*see* Ans. 5; *see also* FF 3). Moreover, each of the interconnects between Ueda's logic gate blocks 1801-1808 is "substantially direct and of minimized length," as claimed and as shown in Figure 20.

It is our view that Ueda's structure (Figure 20) is also capable of performing the claimed functional language of where "at least a second functional element from said plurality of functional elements is rendered substantially direct and of minimized length, *based on said selectively permuting*" (claim 119, emphasis added), even though Ueda's invention selectively permutes bits for an alternate purpose of reducing bus power consumption (*see* FF 1-2). Our reviewing court has determined that the absence of a disclosure relating to function does not defeat a finding of anticipation if all the claimed structural limitations are found in the reference. *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997).

In particular, we note that Appellant's invention accomplishes the stated purpose of minimizing the length of interconnections by "having the

[functional] element's bit order selectively permuted in order to effect substantially straight and direct data paths, or interconnects, having minimized length, between adjacent functional elements." (Spec. p. 8, l. 35 through p. 9, l. 5).

For at least the aforementioned reasons, we find the weight of the evidence supports the Examiner's position. Because we conclude that Appellant has not shown the Examiner erred, we sustain the Examiner's rejection of independent claim 119 as being anticipated by Ueda.

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that Appellant has not met his burden of showing that the Examiner erred in rejecting claims 90-94, 102, 103, and 119 under 35 U.S.C. § 102(b) for anticipation.

However, we conclude that Appellant has met his burden of showing that the Examiner erred in rejecting claims 104-107 and 115-118 under 35 U.S.C. § 102(b) for anticipation.

DECISION

We affirm the Examiner's decision rejecting claims 90-94, 102, 103, and 119.

We reverse the Examiner's decision rejecting claims 104-107 and 115-118.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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