

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PR. CHIDAMBARAM, SRINIVASAN CHAKRAVARTHI, and
HAOWEN BU

Appeal 2008-0364
Application 10/444,054
Technology Center 2800

Decided: April 30, 2008

Before CHARLES F. WARREN, CATHERINE Q. TIMM, and
ROMULO H. DELMENDO, *Administrative Patent Judges*.

DELMENDO, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from a final rejection of all pending claims (claims 20-25, 27, and 39-48). (Final Office Action entered June 14, 2006). We have jurisdiction under 35 U.S.C. § 6(b).

Appellants' invention relates to a layered structure used in forming a complimentary metal-oxide semiconductor (CMOS) device. "The layered structure has a substrate and one or more layers of SiGeC over the substrate[;] . . . the one or more layers of SiGeC have a graded carbon profile." (Spec. ¶ 0011).

Representative claims 20 and 39 read as follows:

20. A layered structure for forming a CMOS device therein, comprising:

a substrate that contains a portion of the CMOS device; and one or more layers of Silicon-Germanium-Carbon (SiGeC) over the substrate, the one or more layers of SiGeC having a graded C profile;

wherein the concentration of C in the one or more layers of SiGeC decreases from a lower portion to an upper portion of the one or more layers of SiGeC.

39. A layered structure for forming a CMOS device therein, comprising:

a substrate that contains a portion of the CMOS device; and two or more layers of Silicon-Germanium-Carbon (SiGeC) over the substrate, the two or more layers of SiGeC having a graded C profile.

The prior art references relied upon by the Examiner to reject the claims on appeal are:

Takagi	6,492,711 B1	Dec. 10, 2002
Suzumura	6,667,489 B2	Dec. 23, 2003

The following rejection is before us for review:

Claims 20-25, 27, and 39-48 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Suzumura in view of Takagi.

ISSUES

Has Appellant shown the Examiner reversibly erred in determining claims 20-25, 27, and 39-48 would have been obvious to one of ordinary skill in the art over the teachings of Suzumura and Takagi?

PRINCIPLES OF LAW

“During patent examination the pending claims must be interpreted as broadly as their terms reasonably allow.” *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989).

“[E]vidence establishing lack of all novelty in the claimed invention necessarily evidences obviousness.” *In re Fracalossi*, 681 F.2d 792, 794 (CCPA 1982).

ANALYSIS

The Rejections of Claims 20-25, 27, and 39-48 Based on 35 U.S.C. § 103 over Suzumura and Takagi.

Appellants submit reasonably specific, but similar, arguments against the Examiner’s rejection as to claims 20 and 39. No other claim is argued separately pursuant to 37 C.F.R. § 41.37(c)(1)(vii), as discussed below. We address Appellants’ arguments accordingly.

Claim 20.

Appellants argue that the prior art does not teach or suggest: 1) “a substrate that contains a portion of the CMOS device” and 2) “a layered structure for forming a CMOS device where the concentration of C in the one or more layers of SiGeC decreases from a lower portion to an upper portion of the one or more layers of SiGeC.” (Br. 13, ll. 6-12). While

Appellants recognize that Suzumura discloses “elements that have a decreasing concentration of C are elements 30 and 34 of FIG. 23,” they contend that this “concentration of C does not decrease from a lower portion to an upper portion of those elements 30 and 34 as advantageously claimed.” (*Id.* 13 bridging to 14). Furthermore, Appellants assert that Suzumura “teaches the use of a substrate containing a bipolar junction device . . . not a CMOS device,” (*Id.* 14, ll. 8-11), and that Takagi “teaches away from the advantageously claimed CMOS structure.” (*Id.* 15, l. 5).

We do not find Appellants’ arguments persuasive. Giving the claim its broadest reasonable reading, as directed by *In re Zletz*, we determine that the scope of claim 20 does not require the CMOS. The claim recites “a layered structure for forming a CMOS device therein.” By using the phrase “structure for forming a CMOS” a functional relationship is set between the claimed layered structure and other elements described in the claim body, such as “a portion of the CMOS device.” With this functional relationship, the claim scope reads on the layered structure by itself because the layered structure is in fact a portion of the CMOS device when combined with the rest of the CMOS device. That is, while the claim recites a layered structure with a “substrate that contains a portion of the CMOS device,” this language only sets out how a substrate would relate to a CMOS, if a CMOS were combined with the layered structure. To construe the claim otherwise would result in an inconsistency with the claim limitation “[a] layered structure for forming a CMOS device therein.”

Here, the Examiner determined Suzumura discloses a heterojunction bipolar transistor (HBT) with SiGeC layers 30 and 34 over a substrate, the layers having a decreasing concentration of carbon from lower portion to

upper portion. (Ans. 3 bridging to 4; Suzumura, Figure 23). The Examiner found the prior art layered structure indistinguishable from the claimed layered structure. Appellants have not demonstrated any reversible error in this determination. Thus, when properly construed, claim 20 is anticipated by and therefore obvious over Suzumura. *In re Fracalossi*, 681 F.2d 792, 794 (CCPA 1982) (“[L]ack of novelty is the ultimate of obviousness. . . . That the rejection here is described as one under [§] 103 is not controlling, for it is not in this case rebuttable by evidence. Here we have the ultimate obviousness-lack of novelty. To recognize that fact is not to replace the rejection with a new one based on anticipation.”).

Even if the claim had explicitly required a CMOS as a necessary part of the claimed structure, the result would not have been different. The Examiner determined that the prior art teaches combining heterojunction bipolar transistors having the claimed SiGeC layers (i.e., the claimed layered structure) with a CMOS. (Ans. 8, ll. 4-18). Here, we agree with the Examiner’s determination that Takagi teaches a SiGeC-HBT capable of integration with a CMOS, (Takagi, col. 24, ll. 47-53), and that combining Takagi’s teachings with Suzumura would have been obvious to one of ordinary skill in the art.

Appellants’ arguments that Suzumura discloses “epitaxial layers only on specific regions . . . but not one or more layers of SiGeC over the entire substrate containing a portion of a CMOS device as advantageously claimed,” (Br. 14 bridging to 15), fail at once because they address limitations not in the claims. There is no claim limitation for layers of SiGeC over the *entire* substrate. *In re Self*, 671 F.2d 1344, 1348 (CCPA

1982) (“[A]ppellant's arguments fail from the outset because . . . they are not based on limitations appearing in the claims.”).

For these reasons, Appellants have not shown that the Examiner reversibly erred in his determination that the prior art discloses the layered structure recited in claim 20.

Claim 39.

Appellants rely on similar arguments as presented with respect to claim 20, above. Appellants argue that the prior art does not teach or suggest “a substrate that contains a portion of the CMOS device” and “two or more layers of Silicon-Germanium-Carbon (SiGeC) over the substrate, the two or more layers of SiGeC having a graded C profile,” (Br. 24, ll. 2-7). The Examiner determined that Suzumura, Figure 23, discloses the substrate, two or more layers of SiGeC over the substrate, and the layers having a graded carbon profile. (Ans. 3 bridging to 4). For the same reasons as discussed above, we agree with the Examiner, and find Appellant’s arguments unpersuasive to show the Examiner reversibly erred in finding the claimed layered structure disclosed in the prior art.

Claims 21-25, 27, and 40-48.

Appellants merely point out what dependent claims 21-25, 27, and 40-48 recite and argue that the prior art does not disclose the claims’ limitations. On the other hand, the Examiner has advanced findings of fact and reasoning supporting a conclusion of obviousness with regard to these claims (Ans. 3-6). Appellants’ mere assertions that a limitation is not in the prior art is not an argument sufficient to warrant separate consideration for patentability because they do not specifically address why the Examiner’s reasoning as to these claims is in error. 37 C.F.R. § 41.37(c)(1)(vii) (2006).

CONCLUSION

Appellants have not shown that the Examiner reversibly erred in determining that one of ordinary skill in the art would have found the subject matter of claims 20-25, 27, and 39-48 obvious over Suzumura and Takagi. Therefore, we affirm the decision of the Examiner to reject appealed claims 20-25, 27, and 39-48.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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TEXAS INSTRUMENTS INCORPORATED
P.O. BOX 655474, M/S 3999
DALLAS, TX 75265