

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HIROSHI FURUTA

Appeal 2008-0561
Application 10/856,999
Technology Center 2800

Decided: May 23, 2008

Before KENNETH W. HAIRSTON, SCOTT R. BOALICK,
and JOHN A. JEFFERY, *Administrative Patent Judges*.
HAIRSTON, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134 from a final rejection of claims 1 to 20. We have jurisdiction under 35 U.S.C. § 6(b).

We will reverse the rejection.

STATEMENT OF THE CASE

Appellant has invented a protection circuit for a semiconductor circuit device. The protection circuit comprises a ring gate to which a first potential is applied, a first impurity diffusion layer formed inside the ring gate, a second impurity diffusion layer formed outside the ring gate, and a shield electrode formed on a substrate to surround the second impurity diffusion layer. A second potential is applied to the shield electrode. One of the first and second impurity diffusion layers is connected to a circuit to be protected, and another impurity diffusion layer receives the first potential (Figures 1 to 3; Spec. 13 to 15).

Claim 1 is representative of the claims on appeal, and it reads as follows:

1. A semiconductor circuit device, comprising:

a protection circuit, the protection circuit, comprising:

a ring gate to which a first potential is applied;

a first impurity diffusion layer formed inside the ring gate;

a second impurity diffusion layer formed outside the ring gate;

and

a shield electrode formed on a substrate to surround the second impurity diffusion layer and to which a second potential is applied, wherein one of the first and second impurity diffusion layers is connected to a circuit to be protected, and another impurity diffusion layer receives the first potential.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

| | | |
|-------|-----------------|---------------|
| Maeda | US 6,204,536 B1 | Mar. 20, 2001 |
| Ker | US 6,690,067 B2 | Feb. 10, 2004 |

The Examiner rejected claims 1 to 20 under 35 U.S.C. § 103(a) based upon the teachings of Ker and Maeda.

ISSUE

Appellant contends *inter alia* that the applied prior art neither teaches nor would have suggested to the skilled artisan a semiconductor circuit device that includes the application of a second potential to a shield electrode and the reception of a first potential by another impurity diffusion layer as set forth in claim 1, and a semiconductor circuit device that is devoid of an element isolation insulating layer between a first protection circuit and a second protection circuit as set forth in claims 13 and 20 (App. Br. 7 to 9). Thus, the issue before us is whether the applied prior art teaches or would it have suggested to the skilled artisan a semiconductor circuit device that receives the claimed potentials, and does not include an element isolation insulating layer between a first protection circuit and a second protection circuit.

FINDINGS OF FACT

As indicated *supra*, the semiconductor circuit device disclosed and claimed by Appellant has a first potential applied to the ring gate and to

another impurity diffusion layer, and a second potential applied to the shield electrode.

Ker describes a substrate-triggered electrostatic discharge (ESD) protection component that comprises a tetragon/square gate 24 to which a first potential VSS is applied (col. 1, ll. 50 to 67; col. 4, ll. 28 to 48), a first impurity diffusion layer 12 formed inside the square gate (col. 4, ll. 22 to 31), a second impurity diffusion layer 20 formed outside the square gate (col. 4, ll. 22 to 31), and a shield/guard ring 18 that surrounds the second impurity diffusion layer (col. 4, ll. 31 to 35). Ker is silent as to the application of a second potential to the shield/guard ring, and the application of the first potential to another impurity diffusion layer.

A plurality of ESD protection components are disclosed in Figure 8 of Ker; however, Ker is silent as to whether the area between the components is devoid of an element isolation layer between the protection components.

According to the Examiner, Maeda describes a semiconductor device that “teaches (e.g. Figures 23 and 24) to form diffusion layer **30**, shield electrodes **10** and an insulating layer **B0** below the diffusion layers and to have the shield electrodes form on a substrate **S1** and in the same layer as the ring gate **102** to permit a voltage drop of serge [sic, surge] voltage without increasing the area of a source/drain layer (Column 8 Lines 9 to 14)” (Ans. 3 and 4).

PRINCIPLES OF LAW

The Examiner bears the initial burden of presenting a prima facie case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). If that

burden is met, then the burden shifts to the Appellant to overcome the prima facie case with argument and/or evidence. *See id.*

The Examiner's articulated reasoning in the rejection must possess a rational underpinning to support the legal conclusion of obviousness. *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006).

ANALYSIS

As indicated *supra*, Ker is silent as to potentials applied to the shield/guard ring and another impurity diffusion layer. Ker is equally silent as to whether the area between the protection components is devoid of an element isolation layer. Thus, even if we assume for the sake of argument that it would have been obvious to one of ordinary skill in the art to provide Ker with the surge protection teachings of Maeda, the combined teachings would still lack the claimed potentials as set forth in claims 1 to 12 and 19, and would lack a plurality of protection circuit components devoid of an element isolation insulating layer between the protection circuit components as set forth in claims 13 to 18 and 20. The Examiner's intended use reasoning is without merit since the potentials set forth in claims 1 to 12 and 19 are applied to the circuit to define the operation of the circuit as a protection circuit (Ans. 4 and 5). Since Figures 23 and 24 of Maeda are directed to a silicon on insulator (SOI) device, we agree with the Appellant's argument that the combined teachings neither teach nor would have suggested to the skilled artisan to avoid the use of an element isolation insulating layer between protection circuit components.

Appeal 2008-0561
Application 10/856,999

CONCLUSION OF LAW

The Examiner has not established the obviousness of claims 1 to 20.

ORDER

The obviousness rejection of claims 1 to 20 is reversed.

REVERSED

KIS

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