

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* LARRY JAY THAYER

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Appeal 2008-0618  
Application 10/156,528  
Technology Center 2100

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Decided: June 30, 2008

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*Before* JAMES D. THOMAS, JOSEPH L. DIXON, and THU A. DANG,  
*Administrative Patent Judges.*

DANG, *Administrative Patent Judge.*

DECISION ON APPEAL

I. STATEMENT OF CASE

Appellant appeals under 35 U.S.C. § 134 from a Final Rejection of claims 1-30. We have jurisdiction under 35 U.S.C. § 6(b).

#### A. INVENTION

According to Appellant, the invention is a system for preventing memory access errors which utilizes a memory chip and logic. The memory chip has a plurality of memory locations. The logic is external to the memory chip and is configured to receive a signal indicative of whether a received memory address is associated with a detected parity error. The logic is further configured to enable the memory chip to access the memory locations based on the memory address if the signal indicates that the memory address is not associated with a detected parity error, and to disable the memory chip from accessing the memory locations based on the memory address if the signal indicates that the received address is associated with a detected parity error (Spec., Abstract).

#### B. ILLUSTRATIVE CLAIM

Claims 1 and 13 are exemplary and are reproduced below:

1. A system for preventing memory access errors, comprising:

a memory chip having a plurality of memory locations; and

logic external to the memory chip, the logic configured to receive a signal indicative of whether a received memory address has a detected parity error, the logic further configured to enable the memory chip to access the memory locations based on the memory address if the signal indicates that the memory address does not have a detected parity error, and to disable the memory chip from accessing the memory locations based on the memory address if the signal indicates that the received address has a detected parity error.

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13. A system for preventing memory access errors, comprising:

memory residing within a memory chip, the memory chip configured to receive a memory address, the memory address comprising chip select information; and

logic configured to receive a signal indicative of whether the memory address has a parity error, the logic further configured to adjust the chip select information based on the received signal.

### C. REJECTIONS

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

DeKarske	US 4,945,512	Jul. 31, 1990
Tsou	US 5,663,969	Sep. 27, 1997

Claims 1-30 stand rejected under 35 U.S.C. § 103(a) over the teachings of DeKarske and Tsou.

We affirm.

### II. ISSUES

The issue is whether Appellant has shown that the Examiner erred in finding that claims 1-30 are unpatentable under 35 U.S.C. § 103(a) over the teachings of DeKarske and Tsou.

### III. FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

#### *Appellant's Invention*

1. Appellant's invention discloses, as prior art, employing parity checking techniques within a memory chip to prevent memory access errors. Address verification logic within each memory chip analyzes the memory addresses received from the memory controller and determines whether or not each of the memory addresses is associated with a parity error. If a received memory address is indeed associated with a parity error, the address verification logic prevents access to the memory within the memory chip, thereby preventing a potential memory access error (Spec. 1-2, para. [0003]).

#### *DeKarske*

2. DeKarske discloses a cache memory which comprises a plurality of cache memory boards and logic circuit and control means mounted on a separated board from said plurality of boards for monitoring data array errors and tag array errors resulting from accessing memory locations in the cache memory and for identifying the exact array where an error has occurred (col. 2, ll. 24-41). In an embodiment, 8K forty bit words of memory which were arranged on four boards 12 and

- a fifth logic board that contains the tag array 28 and an additional board for the cache control logic is provided (col. 4, ll. 16-21; figs. 1A-B).
3. The logic circuitry monitors errors generated when accessing memory addresses in a cache memory and for determining the error status of the memory address (col. 2, ll. 3-7).
  4. The logic circuit and control means includes degrade means coupled to the output of an error status logic means for degrading a portion of the cache memory where an error has been identified (col. 10, ll. 38-42).

*Tsou*

5. Tsou discloses a memory controller parity system that detects both even and odd bit errors in memory addresses and global errors in memory data (Abstract). A concept for error detection includes “Location Stamp” for detecting memory address faults, which employs simple parity checking to detect any combination of errors on an address bus in a memory controller (col. 3, ll. 6-12).
6. The parity-based error detection methods of Tsou can be applied to error detection in off-board Direct Access Storage Device (DASD) system or a Magnetic Tape Storage System (MTSS), wherein the Location Stamp apparatus is disposed within error circuit 76 coupled

to external buffer memory 74 or 78, DASD controller 70 or tape controller 82, and CPU 72 (col. 7, l. 36 to col. 8, l. 6; figs. 6-7).

#### IV. PRINCIPLES OF LAW

##### *35 U.S.C. § 103(a)*

Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'

*KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1734 (2007).

In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," *Id.* at 1739, and discussed circumstances in which a patent might be determined to be obvious. *KSR*, 127 S. Ct. at 1739 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 12 (1966)). The Court reaffirmed principles based on its precedent that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* The operative question in this "functional approach" is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.* at 1740.

The Federal Circuit recently recognized that "[a]n obviousness determination is not the result of a rigid formula disassociated from the consideration of the facts of a case. Indeed, the common sense of those

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skilled in the art demonstrates why some combinations would have been obvious where others would not." *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007) (citing *KSR*, 127 S. Ct. 1727, 1739 (2007)). The Federal Circuit relied in part on the fact that Leapfrog had presented no evidence that the inclusion of a reader in the combined device was "uniquely challenging or difficult for one of ordinary skill in the art" or "represented an unobvious step over the prior art." *Id.* (citing *KSR*, 127 S. Ct. at 1740-41).

One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986).

## V. ANALYSIS

*Claims 1, 3-5, 7, 8, 11, 16, 21, 23, 25, and 27*

Appellant does not provide separate arguments with respect to the rejection of claims 1, 3-5, 7, 8, 11, 16, 21, 23, 25, and 27. Therefore, we select independent claim 1 as being representative of the cited claims. 37 C.F.R. § 41.37(c)(1)(vii).

Appellant argues that DeKarske "fails to suggest any logic for detecting a parity error in the 'received memory address'" and that Tsou "appears to suggest logic for detecting parity errors in memory address but is notably silent as to the location of this logic" (App. Br. 8).

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Appellant appears to be arguing that individually DeKarske and Tsou do not disclose the claimed invention. However, the Examiner has rejected the claims based on the combination of DeKarske and Tsou, and nonobviousness cannot be shown by attacking the references individually.

We agree with the Examiner's finding that DeKarske and Tsou disclose the claimed elements on appeal beginning at page 4 of the Answer and the Examiner's corresponding responsive arguments beginning at page 21 of the Answer.

DeKarske discloses logic circuit and control means mounted external to memory boards, wherein the logic circuitry monitors errors generated when accessing memory addresses (FF 2-3). Tsou discloses a memory controller parity system that detects errors in a memory addresses, which can be applied to error detection in off-board DASD or MTSS systems (FF 5-6). In fact, Appellant's own invention discloses that analyzing the memory addresses received from the memory controller to determine whether or not each of the memory addresses is associated with a parity error was well-known in the art (FF 1).

We agree with the Examiner that the combination of DeKarske and Tsou discloses a logic external to a memory chip, wherein the logic is configured to receive a signal indicative of whether a received memory address has a detected parity error, similar to that of the Appellant's own invention.

Though Appellant argues that DeKarske “fails to suggest any logic for detecting a parity error in the ‘received memory address’” and that Tsou “is notably silent as to the location of this logic” (App. Br. 8), the rejection is based on the combination of DeKarske and Tsou. Thus, the references cannot be attacked individually where the rejections are based on combinations of references. As discussed above, Tsou discloses logic for detecting a parity error in the received memory address (FF 5) and DeKarske discloses a logic external to the memory chip (FF 2-3).

Furthermore, contrary to the Appellant’s assertions, the logic circuitry of DeKarske monitors errors generated when accessing memory addresses in a cache memory and determines the error status of the memory address (FF 3). Similarly, the parity-based error detection methods of Tsou can be applied to error detection in off-board DASD or MTSS systems, external to the logic (FF 6).

Appellant also argues that DeKarske “describes a ‘logic circuit’ for monitoring ‘data array errors’ and ‘tag array errors’” and that such logic circuit is “unlike the alleged ‘parity detection logic’” of Tsou. Accordingly, Appellant argues that “one of ordinary skill in the art would not be motivated to position the alleged ‘logic’ of Tsou in the same location (i.e., external to the ‘memory chip’)” (App. Br. 8-9).

The Examiner’s finding of motivation to combine beginning at page 5 of the Answer complies with the requirements of the above-noted case law.

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DeKarske is directed to an error detection method which includes determining the error status of the memory address, wherein the logic is provided external to the memory chip (FF 2-3). Tsou discloses a method for detecting a parity error in the received memory address, which can be applied to error detection in external, off-board systems (FF 5-6). We thus find that one of ordinary skill in the art would have applied the parity-error detection of Tsou to the teaching of providing an external logic for error detection of DeKarske. We agree with the Examiner that one of ordinary skill in the art would have been motivated to combine these references, since one of ordinary skill in the art would have considered the references to be of analogous art.

Appellant has provided no evidence that incorporating the parity-error detection of Tsou to the external logic for error detection of DeKarske was “uniquely challenging or difficult for one of ordinary skill in the art,” *Leapfrog*, 485 F.3d at 1162, nor has Appellant presented evidence that this incorporation yielded more than expected results. Rather, we find that Appellant’s claimed invention is simply an arrangement of the known teaching of parity-error detection in received memory addresses to a location external to the chip. “[W]hen a patent ‘simply arranges old elements with each performing the same function it had been known to perform’ and yields no more than one would expect from such an arrangement, the combination is obvious.” *KSR*, 127 S. Ct. at 1740 (citing *Sakraida v. AG Pro, Inc.*, 425 U. S. 273, 282 (1976)).

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As to the other recited elements of claim 1, Appellant provides no argument to dispute that the Examiner has correctly shown where all these claimed elements appear in the prior art. Thus, we deem those arguments waived. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2004).

Accordingly, we conclude that the Appellant has not shown that the Examiner erred in rejecting claim 1, and claims 3-5, 7, 8, 11, 16, 21, 23, 25, and 27, falling with claim 1, under 35 U.S.C. § 103(a).

*Claims 2, 9, 13-15, 17-19, 24, and 29*

Appellant does not provide separate arguments with respect to the rejection of claims 2, 9, 13-15, 17-19, 24, and 29. Therefore, we select independent claim 13 as being representative of the cited claims. 37 C.F.R. § 41.37(c)(1)(vii).

Appellant argues that “even if DeKarske is somehow construed to suggest adjusting ‘chip select information’ in a ‘memory address’ in order to ‘degrade’ cache memory, ... there is nothing in DeKarske or Tsou to suggest that memory should be degraded in response to a detection of parity error *in a memory address* transmitted *to* the alleged ‘memory chip’” because “the error [of the claimed invention] is in the ‘memory address’ being transmitted, not the memory being accessed in response to the transmitted ‘memory address’[as taught by DeKarske]” (App. Br. 10-11). However, the Examiner’s finding that DeKarske and Tsou disclose the claimed elements on appeal beginning at page 5 of the Answer and the Examiner’s

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corresponding responsive arguments beginning at page 22 of the Answer meet all of the limitations required by the claims. We agree with the Examiner that the references cannot be attacked individually where the rejections are based on combinations of references.

DeKarske discloses logic external to the memory chip which includes degrade means coupled to the output of an error status logic means for degrading a portion of the cache memory where an error has been identified (FF 2 and 4), and Tsou discloses logic for detecting a parity error in the received memory address (FF 5). We agree with the Examiner that the combination of DeKarske and Tsou discloses the recited feature of a “logic configured to receive a signal indicative of whether the memory address has a parity error, the logic further configured to adjust the chip select information based on the received signal” of claim 13.

In the Reply Brief, Appellant additionally sets forth a new argument that “[t]here is nothing in the cited art to suggest that any ‘chip selection information’ of a ‘memory address’ should be adjusted based on a signal that is indicative of any of the alleged ‘errors’” and thus the cited references do not teach or suggest “adjusting the chip select information based on the received signal”.

However, “[I]t is inappropriate for appellants to discuss in their reply brief matters not raised in . . . the principal brief[ ]. Reply briefs are to be used to reply to matter[s] raised in the brief of the appellee.” *Kaufman Company, Inc. v. Lantech, Inc.*, 807 F.2d 970, 973 n. (Fed. Cir. 1986).

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"Considering an argument advanced for the first time in a reply brief . . . is not only unfair to an appellee . . . but also entails the risk of an improvident or ill-advised opinion on the legal issues tendered." *McBride v. Merrell Dow and Pharms., Inc.*, 800 F.2d 1208, 1211 (D.C. Cir. 1986) (internal citations omitted).

Furthermore, the claims must be given their broadest reasonable interpretation, and limitations cannot to be read into the claims from the specification. Appellant's argument that the teachings of the cited references differ from the claimed invention because "the cited references do not teach or suggest 'adjusting the chip select information based on the received signal'" is not commensurate with the invention that is claimed. That is, such "adjusting" step is not recited in claim 13 under appeal.

We agree with the Examiner's finding that DeKarske discloses the claimed logic that is configured to "adjust the chip select information based on the received signal" beginning at page 12 of the Answer. We agree with the Examiner's that, since "chip select is defined as a ***logical function that gates the inputs and outputs of a memory, i. e. enable or disable***", DeKarske teaches a logic configured "to adjust chip select" since DeKarske "teaches that once an error has been detected the memory will be enabled or disabled accordingly" (Ans. 13).

Accordingly, we conclude that the Appellant has not shown that the Examiner erred in rejecting representative claim 13 and dependent claims 2, 9, 14-15, 17-19, 24, and 29 falling with claim 13 under 35 U.S.C. § 103(a).

*Claims 10, 20, and 22*

Appellant does not provide separate arguments with respect to the rejection of claims 10, 20, and 22. Therefore, we select claim 22 as being representative of the cited claims. 37 C.F.R. § 41.37(c)(1)(vii).

Claims 10, 20, and 22 depend respectively from claims 7, 18, and 1, and thus fall with claims 1, 7, and 18. Appellant argues that claim 22 further comprises “the logic is configured to initiate a retransmission of the received memory address if the signal indicates that the received memory address has a detected parity error.” However, we find that the Examiner’s finding that DeKarske and Tsou disclose the claimed elements on appeal beginning at page 10 of the Answer and the Examiner’s corresponding responsive arguments beginning at page 23 of the Answer meet all of the limitations required by the claims.

As discussed above, Tsou discloses logic for detecting a parity error in the received memory address (FF 5). We agree with the Examiner that it would have been obvious to one of ordinary skill in the art at the time the invention was made that the logic of Tsou is configured to initiate a retransmission of the received memory address if the signal indicates that the received memory address has a detected parity error. We find that such retransmission is merely a predictable use of prior art teachings of parity error detection according to its established functions.

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Accordingly, we conclude that the Appellant has not shown that the Examiner erred in rejecting independent claim 22 under 35 U.S.C. § 103(a) and dependent claims 10, and 20 grouped therewith by Appellant.

*Claims 6, 12, 26, 28, and 30*

Appellant does not provide separate arguments with respect to the rejection of claims 6, 12, 26, 28, and 30. Therefore, we select dependent claim 6 as being representative of the cited claims. 37 C.F.R. § 41.37(c)(1)(vii).

Appellant argues that “the cited art fails to suggest a reason or motivation for locating the alleged ‘logic’ of Tsou external to the alleged ‘memory chip’ of DeKarske but on the same ‘integrated memory module,’ which is ‘detachably coupled’ to a ‘memory controller’” (App. Br. 14).

The Examiner’s finding that DeKarske and Tsou disclose the limitations of the claims on appeal beginning at page 8 of the Answer and the Examiner’s corresponding responsive arguments beginning at page 23 of the Answer comply with the requirements of the above-noted case law.

As set forth by the Examiner, “DeKarske explicitly teaches the error detection monitoring means to be separately mounted from the memory boards” (Ans. 23). We agree with the Examiner that one of ordinary skill in the art would have been motivated to combine DeKarske and Tsou, since one of ordinary skill in the art would have considered the references to be of analogous art. We further agree with the Examiner that it would have been

obvious to one of ordinary skill in the art at the time the invention was made that the logic of Tsou would have been desirable to be on an integrated circuit chip “which may be plugged into the board and removed from the board” (Ans. 24). Such “detachably coupled” integrated circuit chip is merely a predictable use of prior art teachings of a chip according to its established functions.

Appellant has provided no evidence that incorporating the parity-error detection of Tsou to the separately mounted logic for error detection of DeKarske, or to provide a detachably coupled logic, was uniquely challenging or difficult for one of ordinary skill in the art, nor have Appellant presented evidence that this incorporation yielded more than expected results. Rather, Appellant’s invention is simply an arrangement of the known teaching of parity-error detection in received memory addresses to a location separately mounted from and detachably-coupled to the chip.

Accordingly, we conclude that the Appellant has not shown that the Examiner erred in rejecting claim 6 and claims 12, 26, 28, and 30 falling with claim 6 under 35 U.S.C. § 103(a).

#### CONCLUSION OF LAW

(1) Appellant has not shown that the Examiner erred in finding that claims 1-30 are unpatentable under 35 U.S.C. § 103(a) over the teachings of DeKarske and Tsou.

(2) Claims 1-30 are not patentable.

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DECISION

The Examiner's rejection of claims 1-30 under 35 U.S.C. § 103(a) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

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