

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte BUNSHO KURAMORI
and MITSUNORI MURAKAMI

Appeal 2008-0961
Application 10/670,773¹
Technology Center 2800

Decided: September 3, 2008

Before SCOTT R. BOALICK, MARC S. HOFF, and KARL EASTHOM,
Administrative Patent Judges.

HOFF, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134 from a Final Rejection of claims 1-10. We have jurisdiction under 35 U.S.C. § 6(b).

¹ Application filed September 26, 2003. The real party in interest is Oki Electric Industry Co., LTD.

We affirm.

Appellants' invention relates to a substrate voltage generating circuit. The circuit generates a third (substrate) voltage VBB which is lower than first and second voltage levels VDD and VSS (Spec. 1, 3, 5).

Claim 1 is exemplary:

1. A substrate voltage generating circuit comprising:

a first power supply node supplied with a first potential level;

a second power supply node supplied with a second potential level lower than the first potential level;

an output node having a third potential level lower than the second potential level;

a level shift circuit which is coupled between the first power supply node and the output node, which receives an input signal having the first and second potentials level, and which outputs an output signal having the first potential level and the third potential level; and

a switch circuit which connects the second power supply node to the output node in response to the output signal.

No prior art is relied upon by the Examiner in rejecting the claims on appeal.

Claims 1-6 stand rejected under 35 U.S.C. § 112, first paragraph, as lacking enablement.

Claims 1-10 stand rejected under 35 U.S.C. § 112, second paragraph, as failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention.

Appellants contend that the Examiner has not carried his burden, in that he has not explained why undue experimentation would be needed to practice the invention (App. Br. 9); that the Examiner's rejection is misplaced because Appellants' Specification explains how substrate voltage VBB is generated (App. Br. 10); and that the Examiner is incorrect that the voltage at the output node would equal VSS when switches SW1 or SW2 are turned on, because the Specification explains how voltage VBB is attained (App. Br. 12). The Examiner contends that undue experimentation would be required to practice the invention, and that the claims are indefinite because of inconsistency between "an input signal having the first and second potential levels" (claim 1) and first and second transistors "receiving the input signal" (claims 2, 3, and others) (Ans. 4-5).

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Brief (filed December 15, 2006), the Reply Brief (filed July 2, 2007), and the Answer (mailed April 30, 2007) for their respective details.

ISSUE

There are two principal issues in the appeal before us.

The first issue is whether the Examiner erred in holding that the Specification does not reasonably provide enablement for a substrate voltage generating circuit.

The second issue is whether the Examiner erred in holding that the claims are indefinite within the meaning of 35 U.S.C. § 112, second paragraph.

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

The Invention

1. According to Appellants, they have invented a substrate voltage generating circuit. The circuit generates a third (substrate) voltage VBB which is lower than first and second voltage levels VDD and VSS (Spec. 3).

2. Appellants teach that substrate voltage output terminal OUT.vbb is connected to second voltage VSS through either of transistor switches SW1 or SW2, which Appellants disclose are turned ON in alternating fashion (Fig. 1; Spec. 13-15).

3. Appellants' Figure 1 shows that a signal in.101 is applied to input "in" of level shift circuit 101, and an inverted version of that signal, /in.101, is applied to the other input, "/in" (Fig. 1).

PRINCIPLES OF LAW

The standard for determining whether the specification meets the enablement requirement is whether a person skilled in the art can make and use the claimed invention without undue experimentation. *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988). If the examiner's basis for questioning the sufficiency of the disclosure is reasonable, the burden shifts to appellants to come forward with evidence to rebut this challenge. *In re Doyle*, 482 F.2d 1385, 1392 (CCPA 1973).

There are many factors to be considered when determining whether there is sufficient evidence to support a determination that a disclosure does

not satisfy the enablement requirement and whether any necessary experimentation is “undue.” These factors include, but are not limited to:

- (A) The breadth of the claims;
- (B) The nature of the invention;
- (C) The state of the prior art;
- (D) The level of one of ordinary skill;
- (E) The level of predictability in the art;
- (F) The amount of direction provided by the inventor;
- (G) The existence of working examples; and
- (H) The quantity of experimentation needed to make or use the invention based on the content of the disclosure.

Wands, 858 F.2d at 737.

If the claims do not particularly point out and distinctly claim that which applicants regard as their invention, the appropriate action by the examiner is to reject the claims under 35 U.S.C. 112, second paragraph. *In re Zletz*, 893 F.2d 319, 322 (Fed. Cir. 1989). If a rejection is based on 35 U.S.C. 112, second paragraph, the examiner should further explain whether the rejection is based on indefiniteness or on the failure to claim what applicants regard as their invention. *Ex parte Ionescu*, 222 USPQ 537, 539 (BPAI 1984).

ANALYSIS

35 U.S.C. § 112, first paragraph rejection

The Examiner argues that the Specification and drawings do not clearly disclose how “third” (i.e., substrate) voltage VBB, lower than “second” voltage VSS, is generated. The Examiner’s position is that (a) transistor switches SW1 and SW2 are switched on in an alternating manner, such that either one or the other is always on, and (b) as a result, output

terminal OUT.vbb is continuously directly coupled to voltage VSS. Thus, according to the Examiner, the potential at the output terminal is always equal to VSS, and the Specification does not support the recitation of a third voltage, lower than VSS (Ans. 3).

We do not agree with the Examiner's position. First, as noted by Appellants, the Examiner has not addressed the factors for evaluating undue experimentation expressed in *In re Wands, supra* (App. Br. 9). Second, we disagree with the Examiner's contention that undue experimentation would be required to produce a substrate voltage lower than VSS. It is clear from inspection of Appellants' Figure 1 that output terminal OUT.vbb is connected to second voltage VSS through either of transistor switches SW1 or SW2, which Appellants disclose are turned ON in alternating fashion (FF 2). When SW1 or SW2 is turned on by the application of sufficient voltage to its gate, current then conducts between the drain and source of the transistor. There is also some nonzero voltage drop between drain and source, and as a result, the potential at output terminal OUT.vbb will always be less than the potential at VSS, by that nonzero amount. The output node will therefore be at a third potential level (VBB), which is lower than the second potential level (VBB), just as Appellants claim. The skilled artisan would be able to practice the invention simply by following the drawing figures and the description in the Specification. We find that no need for undue experimentation has been shown by the Examiner.

We therefore find error in the rejection of claims 1-6 under 35 U.S.C. § 112, first paragraph.

35 U.S.C. § 112, second paragraph rejection

We select claim 1 as representative of this group, pursuant to our authority under 37 C.F.R. § 41.37(c)(1)(vii).

The Examiner holds the claims to be indefinite because (a) as argued with respect to § 112, first paragraph, it is unclear how the output node in Appellants' invention produces a third potential level lower than the second potential level (Ans. 4), and (b) claim 1's recitation of "an input *signal* having the first *and* second potential levels" (emphasis added) is confusing, especially when considered in contrast with claim 2 (as well as other claims), which recites first and second transistors of the first conductivity type which have "a gate receiving *the input signal*" (emphasis added) (Ans. 4-5). Appellants argue that the claims are not confusing because the Specification explains that "the input signal," having first and second potential levels VDD and VSS, is supplied to inputs in.101 and /in.101 of level shift circuit 101, and inputs in.101 and /in.101 respectively are supplied to the first and second transistors of the first conductivity type in the level shift circuit (App. Br. 13).

Appellants urge us to construe claim 1's requirement of "an input signal having the first and second potential levels" according to the explanation in their Specification, which shows that a signal in.101 is applied to input "in" of level shift circuit 101, and an inverted version of that signal, /in.101, is applied to the other input, "/in" (FF 3). The next sentence of Appellants' claim, however, recites "an output signal having the first potential level and the third potential level." Appellants disclose that *this* identically-worded phrase should be accorded a *different* meaning, *i.e.*, that

there is a *single* output signal line whose potential alternates between the first level and the third level. Claim 2 then refers to two discrete transistors, each having a gate receiving *the* input signal.

We are not persuaded by Appellants' position. If "an input signal", singular, "having the first and second potential levels" is meant to refer to two distinct "wires," as it were, each at a different potential level, as recited in claim 1, that construction is not consistent with the language of claim 2, which calls for "a" (singular) first transistor which has "a" (singular) gate receiving "the" (singular) "input signal," and "a" second transistor which has "a" gate receiving "the" input signal. Appellants' suggested interpretation of "an input signal" as corresponding to two distinct "wires" is also inconsistent with their interpretation of "an output signal," in the very next line of claim 1, as corresponding to a single "wire." We agree with the Examiner that Appellants are not entitled simultaneously to assign two inconsistent meanings to the same phrase.

We therefore find the language of claim 1 to be indefinite, and we sustain the Examiner's rejection of claim 1, as well as that of claims 2-10 not separately argued, under 35 U.S.C. § 112, second paragraph.

CONCLUSION OF LAW

We conclude that Appellants have shown that the Examiner erred in rejecting claims 1-6 under 35 U.S.C. § 112, first paragraph. We further conclude that Appellants have not shown that the Examiner erred in rejecting claims 1-10 under 35 U.S.C. § 112, second paragraph.

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DECISION

The Examiner's rejection of claims 1-10 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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Stuebaker & Brackett PC
1890 Preston White Drive
Suite 105
Reston, VA 20191