

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KLAUS-PETER BEHRENS, MARKUS ROTTACKER, and
JOERG-WALTER MOHR

Appeal 2008-1236
Application 10/032,513
Technology Center 2600

Decided: July 22, 2008

Before MAHSHID D. SAADAT, ROBERT E. NAPPI,
and KARL D. EASTHOM, *Administrative Patent Judges*.

NAPPI, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 6(b) of the final rejection of claims 1 through 11.

We affirm the Examiner's rejection of these claims.

INVENTION

The invention is directed to synchronizing data flow between a device being tested which operates at one clock rate and the test equipment which operates at a different clock rate. See pages 1 and 2 of Appellants'

Specification. Claim 1 is representative of the invention and reproduced below:

1. A testing unit for testing a device under test (DUT), comprising:
a signal generator that applies a stimulus signal to the DUT,
a receiving unit that receives a response signal from the DUT on the applied stimulus signal; and
a synchronizing unit that synchronizes a data flow of the response signal between the DUT and the receiving unit;
wherein the synchronizing unit receives a first clock signal from the DUT and a second clock signal from the testing unit; and
wherein the synchronizing unit includes:
a buffer for buffering data;
a write unit for writing data from the DUT into the buffer,
wherein the first clock signal controls a write access onto the buffer; and
a read unit for reading out data from the buffer to be provided to the receiving unit, wherein the second clock signal controls a read access onto the buffer.

REFERENCES

Alston	US 6,055,285	Apr. 25, 2000
Farwell	US 6,324,664 B1	Nov. 27, 2001

REJECTION AT ISSUE

Claims 1 through 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Farwell and Alston. The Examiner's rejection is on pages 3 through 10 of the Answer.

Throughout the opinion, we make reference to the Brief (received April 16, 2007), Reply Brief (received August 10, 2007) and the Answer (mailed June 14, 2007) for the respective details thereof.

ISSUES

Appellants argue on pages 7 and 8 of the Brief that the Examiner's rejection of claims 1 through 11 is in error. Appellants state that independent claim 1 recites that the first clock signal controls a write access into the buffer and the second clock signal controls read access to the buffer. Appellants state that the Examiner "recognizes that the Farwell et al. patent does not specifically disclose that a first clock signal controls a write access into a buffer, and a second clock signal controls a reads access onto the buffer." Brief 8. Appellants argue that as Farwell's system accommodates asynchronous clocks, there is no reason that one would modify Farwell to include the synchronization circuit of Alston. Brief 8.

Thus Appellants' contentions present us with the issue of whether the Examiner erred in combining Farwell with the teachings of Alston.

FINDINGS OF FACT

1. Farwell teaches a system for testing a circuit. The circuit being tested has a scan path having serially coupled flip flops. The system receives test data from an external source. The system includes a control circuit which receives test data from and provides output data to an external source (item 33). Abstract.
2. Farwell teaches that the system clock (SYSCLK) clocks the scan path and the combinatorial logic (the device under test). This clock controls the input of data into memory 18 (input memory). The scan path also controls the input of data from the scan path to the memory 25(output memory). Col. 4, ll. 24-31 and ll. 38-43.

3. Farwell teaches that a second clock “TEST CLOCK” is used to read the output memory. Col. 4, ll. 44-45.
4. Farwell also teaches that when the output memory (item 25) is read a flag is set which allows the input memory (item 18) to read the next piece of data. Col. 4, ll. 46- 55.

PRINCIPLES OF LAW

On the issue of obviousness, the Supreme Court has recently stated that “[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.”

KSR Int’l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1739 (2007).

When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. . . . [A] court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

Id. at 1740. “One of the ways in which a patent’s subject matter can be proved obvious is by noting that there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent’s claims.” *Id.* at 1742.

37 C.F.R. § 41.37 (c)(1)(vii) states:

For each ground of rejection applying to two or more claims, the claims may be argued separately or as a group. When multiple claims subject to the same ground of rejection are argued as a group by appellant, the Board may select a single claim from the group of

claims that are argued together to decide the appeal with respect to the group of claims as to the ground of rejection on the basis of the selected claim alone. Notwithstanding any other provision of this paragraph, the failure of appellant to separately argue claims which appellant has grouped together shall constitute a waiver of any argument that the Board must consider the patentability of any grouped claim separately.... A statement which merely points out what a claim recites will not be considered an argument for separate patentability of the claim.

ANALYSIS

Appellants' arguments have not persuaded us of error in the Examiner's rejection of claims 1 through 11. Initially we note that Appellants have stated that "[c]laims 1-11 stand or fall together" and have not provided arguments separately addressing the claims. Brief 7. Thus in accordance with 37 C.F.R. § 41.37 (c)(1)(vii), claims 1 through 11 are grouped together and we select claim 1 as representative.

Claim 1 recites "a write unit for writing data from the DUT into the buffer, wherein the first clock signal controls a write access onto the buffer; and a read unit for reading out data from the buffer to be provided to the receiving unit, wherein the second clock signal controls a read access onto the buffer." Thus, the scope of claim 1 includes two clock signals: one controls writing of data to the buffer and the other reading data from the buffer. The Examiner finds that Farwell's memory item 25 meets the claimed buffer. Answer 3. This finding is not contested by Appellants and we concur with the Examiner's finding. The Examiner also finds that Farwell teaches that there are two clock signals used with the synchronizing unit. Answer 3. We concur with this finding by the Examiner. Facts 2 and

3. Further, the Examiner states that Farwell does not disclose the details of the first clock signal controlling a write access and the second control signal controlling the read access. Answer 4. While we agree with the Examiner's statement that Farwell does not disclose the specific details of how the clocks control the reading and writing to the buffer, we do find that Farwell identifies that the two clocks control the writing and reading of data to the buffer. Specifically, Farwell teaches that the system clock controls the flow of data written to the output memory item 25 (claimed buffer), and that a test clock controls the flow of data read out of the output memory. Facts 2 and 3. Thus, Farwell alone appears to suggest that there are two clock signals, one controls writing of data to the buffer and the other reading data from the buffer. Nonetheless, the Examiner finds, on page 4 of the Answer that Alston teaches the limitation of two clock signals where one controls writing of data to the buffer and the other reading data from the buffer. Appellants have not contested this finding, but rather the Examiner's holding that it would have been obvious to combine the teachings of Farwell and Alston.

Alston teaches that the prior art synchronization circuits operate such that data can only be transferred one unit at a time, thus, "one circuit places the unit of data on a transmission bus; sets an indicator that informs the other circuit that the unit of data is ready; waits until the other circuit receives the unit of data and acknowledges receipt." Col. 1, ll. 50-54. Alston identifies that though this may work for some systems, it is not efficient for transmitting large amounts of data, thus, Alston's invention provides more efficient transfer of large amounts of data. Col. 1, ll. 56-60. We note that Farwell teaches a system similar to the inefficient system discussed in Alston, where one circuit awaits the indication from the other circuit that the

data is acknowledged. Fact 4. The Examiner has found that it would have been obvious to use the synchronization circuit of Alston in the test circuit of Farwell. Answer 4. We concur with the Examiner as we consider the use of Alston's circuit in Farwell to be nothing more than using known techniques for their known purposes. *See KSR at 1739*. In this case, Alston specifically teaches that his device improves the efficiency of synchronization circuits such as that used by Farwell. Appellants' argument, on pages 2 and 3 of the Reply Brief, that the combination would change the operation of elements of Farwell's device, does not persuade us of error in combining the references as any modification will change the operation of elements of the device, the question is whether the change would be obvious. In this case, we find that the change is obvious. As we are not persuaded of error in the Examiner's rejection by Appellants' arguments, we sustain the Examiner's rejection of claims 1 through 11 under 35 U.S.C. § 103(a).

CONCLUSION

Appellants' arguments have not persuaded us of error in the Examiner's rejection of claims 1 through 11 under 35 U.S.C. § 103(a).

The decision of the Examiner is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

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AFFIRMED

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