

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* DEBENDRA DAS SHARMA

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Appeal 2008-2207  
Application 10/444,614<sup>1</sup>  
Technology Center 2600

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Decided: September 29, 2008

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Before JOSEPH F. RUGGIERO, JOHN A. JEFFERY, and MARC S.  
HOFF, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

Appellant appeals under 35 U.S.C. § 134 from a non-final rejection of claims 1, 3-8, 17, 19-24, 33, and 35.<sup>2</sup> We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

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<sup>1</sup> Application filed May 23, 2003. The real party in interest is Hewlett-Packard Development Company, L.P.

<sup>2</sup> Claims 2, 14-16, 18, 30-32, 34, and 36-55 have been cancelled. Claims 9-13 and 25-29 stand objected to as dependent upon a rejected base claim (App. Br. 3).

Appellant's invention relates to communication between nodes in a network computer system, specifically "initializing credit in a queue flow control system" (Spec. 1). During initialization, the credit register at a sender node is loaded with a zero, and thus cannot send any transactions. The debit register, at a destination node, is loaded with the maximum credits representing the size of its queue. The debit register then releases its credits back to the sender node, enabling the sender node to send transactions (Spec. 6).

Claim 1 is exemplary:

1. A method for initializing credit in a credit register used for flow control that is resident on a first node of a multinode computer system, the method comprising the steps of:  
loading an initial credit value into a debit register resident on a second node of the multinode computer system  
transferring the initial credit value from the debit register into the credit register by using operational mechanisms of the system; wherein the initial credit value is equal to a size of a queue that is resident on the second node and receives information from the first node.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Sugawara	US 5,852,602	Dec. 22, 1998
Barkey	US 6,044,406	Mar. 28, 2000
Abdalla	US 6,154,794	Nov. 28, 2000
Sakagawa	US 6,421,321 B1	Jul. 16, 2002
Lynch	US 6,574,294 B1	Jun. 3, 2003

Claims 1, 17, and 33 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Sugawara.

Claims 3, 19, and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sugawara in view of Lynch or Admitted Prior Art (APA).

Claims 4 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sugawara in view of Adballa.

Claims 5, 7, 8, 21, 23, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sugawara in view of Barkey.

Claims 6 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sugawara in view of Barkey and Sakagawa.

Rather than repeat the arguments of Appellant or the Examiner, we make reference to the Appeal Brief (filed May 18, 2007), the Reply Brief (filed October 9, 2007), and the Answer (mailed August 20, 2007) for their respective details.

### ISSUES

There are two principal issues in the appeal before us.

The first issue is whether the Examiner erred in holding that Sugawara teaches loading an initial credit value equal to a size of a queue resident on a receiving (second) node which receives information from a sending (first) node, into a debit register on the second node, then transferring that value into a credit register on the first node.

The second issue is whether the Examiner erred in holding that Sugawara in combination with Barkey renders obvious decrementing the debit register on the second node by the initial credit value when that credit value is transferred to the credit register on the first node.

## FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

### *The Invention*

1. According to Appellant, he has invented a system and method for communication between nodes in a network computer system, specifically “initializing credit in a queue flow control system” (Spec. 1). During initialization, the credit register at a sender node is loaded with a zero, and thus cannot send any transactions. The debit register, at a destination node, is loaded with the maximum credits representing the size of its queue. The debit register then releases its credits back to the sender node, enabling the sender node to send transactions (Spec. 6).

2. Appellant admits that it is known in the prior art that “the credit and debit registers are set to zero” (Spec. 4:18-19).

### *Sugawara*

3. Sugawara teaches a credit control method and system for an ATM communication apparatus (col. 2, ll. 35-37).

4. Sugawara teaches that a packet containing an initial credit value corresponding to the maximum number of bursts which can be received by the data receiving side is sent from the receiving side (T2 in Fig. 1B) to the sending side (T1 in Fig. 1B) (col. 1, ll. 34-37; col. 8, ll. 14-23).

5. Once this initial credit value is received, the sending node T1 may begin sending a number of packets equal to that initial credit value (col. 8, ll. 23-25).

6. Sugawara teaches checking the presence/absence and type of input control data from the input buffer controller (col. 9, ll. 56-58).

7. If the control input is reception of initial credit, the credit controller stores the initial credit value as a credit value indicating a number of transmittable packets (col. 10, ll. 1-4). If the control input is reception of new credit, the credit controller adds the credit values stored in the memory and instructs the output buffer controller to send a data packet (col. 10, ll. 9-12).

*Lynch*

8. Lynch teaches the exchange of high-speed data streams between two digital computing devices, one or both of which lacks direct memory access (col. 3, ll. 46-48).

9. Lynch teaches that “[t]he flow control credit is a 16-bit quantity which starts at zero upon initialization” (col. 9, ll. 40-41).

*Sakagawa*

10. Sakagawa teaches a communications network in which a packet is transferred from a first device to a second device through a third device. A determination means provided in one of the first and second devices determines whether to set a path directly connecting the first device to the second device. An instruction means provided in the other of the two devices instructs the communications network to set the path (col. 6, ll. 24-34).

*Adballa*

11. Adballa teaches a method and apparatus for controlling the flow of information to an input/output unit within a computer controlled input/output system (col. 2, l. 67 – col. 3, l. 3).

12. Adballa teaches a “reset load circuit” 340 which, when invoked, loads an initial value within credit counter 315 (Adballa col. 7, ll. 9-13).

*Barkey*

13. Barkey teaches a “credit-based method for controlling data communications in a closed loop system comprising a sender and a receiver coupled by a link” (col. 2, ll. 39-42).

PRINCIPLES OF LAW

Anticipation of a claim requires a finding that the claim at issue reads on a prior art reference. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed. Cir. 1999) (quoting *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 781 (Fed. Cir. 1985)).

Analysis of whether a claim is patentable over the prior art under 35 U.S.C. § 102 begins with a determination of the scope of the claim. We determine the scope of the claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004). The properly interpreted claim must then be compared with the prior art.

In an appeal from a rejection for anticipation, the Appellant must explain which limitations are not found in the reference. *See Gechter v. Davidson*, 116 F.3d 1454, 1460 (Fed. Cir. 1997) (“[W]e expect that the Board's anticipation analysis be conducted on a limitation by limitation basis, with specific fact findings for each *contested* limitation and satisfactory explanations for such findings.”)(emphasis added). *See also In*

*re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) (“On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.”) (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

“Section 103 forbids issuance of a patent when ‘the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.’” *KSR Int’l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1734 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) where in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). *See also KSR*, 127 S.Ct. at 1734 (“While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.”)

In *KSR*, the Supreme Court emphasized “the need for caution in granting a patent based on the combination of elements found in the prior art,” *id.* at 1739, and discussed circumstances in which a patent might be determined to be obvious. In particular, the Supreme Court emphasized that “the principles laid down in *Graham* reaffirmed the ‘functional approach’ of *Hotchkiss*, 11 How. 248.” *KSR*, 127 S.Ct. at 1739 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 12 (1966) (emphasis added)), and reaffirmed

principles based on its precedent that “[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” *Id.* The Court explained:

When a work is available in one form of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

*Id.* at 1740. The operative question in this “functional approach” is thus “whether the improvement is more than the predictable use of prior art elements according to their established functions.” *Id.*

## ANALYSIS

### *Claims 1, 17, and 33*

We select claim 1 as representative of this group, pursuant to our authority under 37 CFR § 41.37(c)(1)(vii).

Appellant argues that Sugawara does not teach initializing credit in a credit register (Reply Br. 4), nor that the initial credit value is equal to a size of a queue that is resident on the second node and receives information from the first node (App. Br. 6).

We are not persuaded by Appellant’s arguments. Sugawara teaches that a packet containing an initial credit value corresponding to the maximum number of bursts which can be received by the data receiving side is sent from the receiving side (T2 in Fig. 1B) to the sending side (T1 in Fig.

1B) (FF 4). Once this initial credit value is received, the sending node T1 may begin sending a number of packets equal to that initial credit value (FF 5).

Sugawara thus teaches all the features of claim 1. As a result, we do not find error in the Examiner's rejection of claims 1, 17, and 33 under 35 U.S.C. § 102(b).

*Claims 3, 19, and 35*

We select claim 3 as representative of this group, pursuant to our authority under 37 CFR § 41.37(c)(1)(vii).

Appellant argues that Lynch fails to teach "loading the credit register with zero prior to the step of transferring," as claim 3 requires, because Lynch simply sets a value at the beginning, rather than the claimed loading (App. Br. 8).

We do not find Appellant's position persuasive. The Examiner relies on either Lynch or Appellant's Admitted Prior Art (APA), in the alternative, to supply the teaching of "loading the credit register with zero" missing from Sugawara. Lynch teaches, in pertinent part, that "[t]he flow control credit is a 16-bit quantity which starts at zero upon initialization" (FF 9). The APA teaches that "the credit and debit registers are set to zero" (FF 2). In both cases, a memory location or register is caused to attain a certain value, i.e. zero. Appellant argues that "[t]here is a difference between loading and setting" (App. Br. 8), but never articulated the nature of the difference nor cited any authority to establish the difference. We therefore concur in the Examiner's finding that either or both of Lynch and APA teach the limitation at issue. With respect to Appellant's argument that the Examiner

lacks motivation to combine, we concur in the Examiner's conclusion in the Answer, which is unrebutted in the Reply Brief, that it would have been obvious to load a zero in order to synchronize the credit and debit registers (Ans. 5).

Thus, we do not find error in the Examiner's rejection of claims 3, 19, and 35 under 35 U.S.C. § 103(a).

*Claims 4 and 20*

We select claim 4 as representative of this group, pursuant to our authority under 37 CFR § 41.37(c)(1)(vii).

Appellant argues the combination of Sugawara and Adballa does not teach the invention recited in claim 4. Appellant argues that Adballa's teaching of a "reset load circuit" which, when invoked, loads an initial value within credit counter 315 (FF 12), does not equate to "the step of loading is performed after a reset condition has been lifted," because the cited section of Adballa "clearly shows that the loading occurs as part of the reset condition," which "is not the same as loading after a reset condition has been lifted" (App. Br. 10).

The Examiner essentially argues that Adballa inherently teaches the limitation at issue, because "reset process and loading process cannot be performed at the same time," and that "[l]oading must be performed after resetting" (Ans. 9). We are not persuaded by the Examiner's position. We have reviewed Adballa and, apart from the labeling of element 340 as the "reset load circuit," Adballa contains no teaching of any "reset" of any hardware, as the term is understood by those having ordinary skill in the art.

Because Adballa does not teach any reset condition, it is necessarily the case that Adballa also does not teach the lifting of any reset condition.

Because the combined teachings of the references do not meet all the limitations of claim 4, we do not sustain the Examiner's rejection of claims 4 and 20 under 35 U.S.C. § 103(a).

*Claims 5, 8, 21, and 24*

We select claim 5 as representative of this group, pursuant to our authority under 37 C.F.R. § 41.37(c)(1)(vii).

Appellant argues that the Examiner's asserted combination of Sugawara and Barkey is improper because the Examiner's stated motivation for combining the references is circular (App. Br. 10).

We are not persuaded by Appellant's position. The Examiner concludes that it would have been obvious to decrement the debit register by the initial credit value (i.e., an amount equal to the amount added to the credit register), as disclosed by Barkey, in order to "update the debit register to reflect the current state of the debit register" (Ans. 10). While the Examiner's phrasing may not accurately reflect his meaning, we concur in the Examiner's further conclusion that "if the debit register is not decremented as the credit value is sent to the first node, then the credit based flow control system would not work at all" (*id.*). Credit-based flow control systems such as Sugawara and Barkey are intended to keep a sending node from sending more data packets than the queue at the receiving node can handle. For that to occur, one must decrement the debit register at the receiver concurrently with the incrementing of the credit register at the sender.

We therefore do not find error in the Examiner's rejection of claims 5, 8, 21, and 24 as being unpatentable under 35 U.S.C. § 103(a).

*Claims 7 and 23*

We select claim 7 as representative of this group, pursuant to our authority under 37 C.F.R. § 41.37(c)(1)(vii).

Appellant argues that the Examiner failed to establish a prima facie case of obviousness because Sugawara does not teach inspecting a packet to determine whether the packet includes credits for the first node, as claim 7 requires (App. Br. 11).

We find Appellant's position unpersuasive. We concur with the Examiner's finding that Sugawara *does* teach this limitation (Ans. 10). Sugawara teaches checking the presence/absence and type of input control data from the input buffer controller (FF 6). If the control input is reception of initial credit, the credit controller stores the initial credit value as a credit value indicating a number of transmittable packets (FF 7). If the control input is reception of new credit, the credit controller adds the credit values stored in the memory and instructs the output buffer controller to send a data packet (FF 7).

We therefore do not find error in the Examiner's rejection of claims 7 and 23 as being unpatentable under 35 U.S.C. § 103(a).

*Claims 6 and 22*

We select claim 6 as representative of this group, pursuant to our authority under 37 C.F.R. § 41.37(c)(1)(vii).

Appellant argues that the Examiner's reasoning to combine Sugawara with Barkey and Sakagawa is circular, and thus that the Examiner has not articulated a proper motivation for making the asserted combination.

We observe that Appellant appears to have inadvertently repeated their arguments related to claim 5 in this section of the Brief, and that the Examiner, noting this, did not respond substantively to Appellant's position (App. Br. 11-12; Ans. 10).

The Examiner concluded that it would have been obvious to modify Sugawara and Barkey to include determining whether a packet is destined for a first node; forwarding the packet to another node, if the packet is not destined for the first node; and processing the packet, if the packet is destined for the first node, "so that any packet that does not belong to the receiving node will be forwarded to its destination" (Ans. 8). Taking the teachings of Sugawara, Barkey, and Sakagawa together, we agree with the Examiner that forwarding a packet, not destined for a given node, to the proper node is known in the art. Such forwarding is desirable because senders and receivers of data clearly want their data to arrive at its intended destination. Modifying Sugawara and Barkey to include the forwarding disclosed in Sakagawa would have been obvious, because such forwarding increases the likelihood that data packets will ultimately be routed to their intended destinations. Further, given that Sakagawa shows that such forwarding is known, we find that this combination of known elements would have produced the predictable result that data packets will tend to arrive where intended. *See KSR*, 127 S. Ct. at 1739.

We therefore do not find error in the Examiner's rejection of claims 6 and 22 as being unpatentable under 35 U.S.C. § 103(a).

#### CONCLUSION OF LAW

We conclude that Appellant has shown that the Examiner erred in rejecting claims 4 and 20. On the record before us, claims 4 and 20 have not been shown to be unpatentable.

We further conclude that Appellant has not shown that the Examiner erred in rejecting claims 1, 3, 5-8, 17, 19, 21-24, 33, and 35. Claims 1, 3, 5-8, 17, 19, 21-24, 33, and 35 are not patentable.

#### DECISION

The Examiner's decision rejecting claims 1, 3, 5-8, 17, 19, 21-24, 33, and 35 is affirmed. The Examiner's decision rejecting claims 4 and 20 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

Appeal 2008-2207  
Application 10/444,614

AFFIRMED-IN-PART

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