

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOSEPH E. GEUSIC,
PAUL A. FARRAR
and ARUP BHATTACHARYYA

Appeal 2008-2697
Application 10/931,593
Technology Center 2800

Decided: September 19, 2008

Before JOSEPH F. RUGGIERO, ROBERT E. NAPPI,
and KARL D. EASTHOM, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Final Rejection of claims 1-16. Claims 17-23 have been withdrawn from consideration. No

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other claims are pending (*see* App. Br. 2, Final Office Action, mailed August 24, 2006). We have jurisdiction under 35 U.S.C.

§ 6(b).

We affirm-in-part.

Appellants' invention relates to an insulator having at least one void formed within the solid structure. The void(s) decrease the dielectric constant of the otherwise solid structure. (*See* Spec. 4, Figs. 2F, 3C).

Claim 1 is illustrative of the invention and reads as follows:

1. An integrated circuit insulator structure, comprising:
 - a solid structure of an insulator material; and
 - a precisely-determined arrangement of at least one void formed within the solid structure,wherein the precisely-determined arrangement of at least one void within the solid structure lowers an effective dielectric constant of the insulator structure.

The Examiner relies on the following prior art references to show unpatentability:

Nishiwaki	US 6,013,970	Jan. 11, 2000
Moslehi	US 6,016,000	Jan. 18, 2000
Aoi	US 6,387,824 B1	May. 14, 2002

We additionally rely on:

Farrar	US 6,077,792	June 20, 2000
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Claims 1-6, 8 and 12-14 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Aoi.

Claims 1, 6, and 7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Nishiwaki.

Claims 1 and 9-11 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Moslehi.

Claims 15 and 16 stand rejected under 35 U.S.C. § 103(a) as being obvious over Aoi.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the Brief and Answer for the respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived. 37 C.F.R. § 41.37(c) (1) (vii).

FINDINGS OF FACT (FF)

1. Aoi discloses forming a porous insulator of silicon dioxide having fine holes with diameters controlled on the molecular level. The resultant porous insulator has a reduced dielectric constant of 1.7 as compared to 3.2 as measured in a starting film comprising an organic-inorganic hybrid film from which the porous silicon dioxide film was produced. (Col. 6, l. 66 to col. 7, l. 4; col. 7, l. 23-32, col. 7, l. 59-62).

2. Aoi discloses controlling the molecular level diameter of fine holes “so that the dielectric constant of the porous film is reduced reliably” (col. 4, ll. 3-7).

3. Aoi discloses a structure having one porous insulator 26 having a greater porosity and lesser dielectric constant as compared to another such insulator 25 formed below the first insulator, with each insulator located in

specific locations relative to a metal contact structures 27. (Col. 11, l. 25 to col. 12, l. 43; Fig. 4c).

4. Nishiwaki discloses “an amorphous porous gel thin film . . . in a thickness of 0.4 um. . . .” (Col. 3, ll. 61-62).

5. Moslehi discloses different arrays of patterned windows (squares, rectangles, circles) having specific sizes and locations etched in a dielectric. (Col. 12, l. 51 to col. 13, l. 25; Figs. 9-13).

PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) (“On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence *of prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.”) (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

Appellants may sustain this burden by showing that the prior art reference relied upon by the Examiner fails to disclose an element of the claim. It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. *See In re King*, 801 F.2d 1324, 1326 (Fed. Cir. 1986); *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984).

Under § 103, if the claimed subject matter cannot be fairly characterized as involving the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement, a holding of obviousness can be based on a showing that “there was an apparent reason to combine the known elements in the fashion claimed.” *KSR Int’l v. Teleflex, Inc.*, 127 S. Ct. 1727, 1740-41 (2007). Such a showing requires:

“ . . . some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness” . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

Id. at 1741 (*quoting Kahn*, 441 F.3d at 987).

ANALYSIS

Anticipation rejection based upon Aoi

Appellants’ arguments regarding the anticipatory rejection under Aoi of claims 1-6, 8 and 12-14 focus on independent claims 1 and 13 without distinction.¹ (App. Br. 6). Similarly, Appellants’ arguments regarding the anticipatory rejections of claims 1, 6, and 7, and claims 1 and 9-11,

¹ In addition to their arguments for claim 1, Appellants merely recite certain limitations of independent claim 13 and assert that they are missing (App. Br. 6). Such a recitation and assertion do not constitute a separate argument for patentability. (*See* 37 C.F.R. § 41.37(c) (1) (vii)). We similarly interpret Appellants’ Reply Brief as grouping claims 1 and 13 together, because the response generally refutes the Examiner’s finding of precise shapes and locations. We also find no basis in the rules for regrouping the claims in the Reply Brief.

respectively under Nishiwaki and Moslehi, also focus on independent claim 1. (App. Br. 6-8). Therefore, we select claim 1 as the representative claim for each of the separate anticipatory rejections.

Regarding Aoi, Appellants dispute the Examiner's finding that Aoi discloses "a precisely-determined arrangement of at least one void formed within the solid structure" as recited in claim 1 (*See* App. Br. 6). The thrust of Appellants arguments throughout the Brief and Reply Brief is that Aoi's holes are randomly located, and as such, are not in "a precisely-determined arrangement" as recited in claim 1.

The Examiner set forth three separate reasons as to why Appellants' argument is not persuasive:

First, the Examiner found that since the voids are located in a solid "static" structure, they are in a precisely determined arrangement (*see* Ans. 8). "After a porous material layer has been made the voids will not move to another location because the layer is in [a] solid state." (Ans. 8). Appellants do not dispute the factual basis for the determination. Rather, in response, Appellants point to their Specification and "submit[] that the Examiner is incorrect in stating on page 8 that the 'voids can be considered to be formed at specific[] locations since they are static', and submit[] that it is clear to one of ordinary skill in the art that the presently claimed voids are located at a specified depth and radius based upon the etched cylindrical holes as shown in figures 2-4, and as located by the photoresist mask location." (Reply Br. 2-3).

Appellants' argument is not persuasive. It does not respond to the Examiner's determination that Aoi's voids, once formed, are precisely determined. That is, because there is no dispute about whether the void

locations are fixed in the solid after formation thereof (albeit arguably at random locations within the solid during formation), it follows that such locations are precisely-determined at such random locations. In other words, we find that one can pinpoint, (i.e., precisely determine), the exact location and/or size of at least one void in the solid after the voids have been fixed in place.

Appellants' reliance on the Specification as supporting the precise determination of void locations prior to formation, or as supporting voids empty of unwanted metal (Reply Br. 3), simply fails to address the Examiner's reasonable determination. Even assuming as correct Appellants' related assertion that metal flows into some of Aoi's voids, we fail to see how this defeats the finding that Aoi's remaining at least one void(s) is (are) precisely-determined as fixed or static. Accordingly, Appellants have failed to convince us of error in the Examiner's determination.

Second, as the Examiner generally reasoned (*compare* Ans. 8), Appellants merely disclose, but do not claim, a set distance between voids, or a location of at least one void(s). Aoi's voids have a controlled diameter (FF 1, 2). Moreover Appellant claims "at least one void." As such, since Aoi discloses voids having a controlled diameter within a solid structure, any one such void constitutes "a precisely-determined arrangement of at least one void formed within the solid structure," regardless of the void location within the structure, because such a void and its diameter have been precisely determined to be within the structure.

Third, as the Examiner found, Aoi's dielectric constant is precisely determined by the voids within the structure. (*Compare* Ans. 7). Appellants do not dispute this finding. As such, because we concur with the Examiner

that Aoi's dielectric constant is precisely determined by the void size and number (*see* FF 1-3), such a determination constitutes "a precisely-determined arrangement of at least one void formed within the solid structure," as set forth in the claim. Under a related interpretation, we also alternatively find that the group of voids 26 have a precisely fixed location with respect to another group of voids 25 in the same insulating structure of Figure 4c (FF 3). Therefore, Aoi's Figure 4c arrangement also meets the claim.

Finally, we note that Appellants' arguments imply that the claims are patentable because precise distances and/or shapes and/or sizes between and of voids that already exist in prior art structures have been fixed or pre-determined by Appellants' disclosed process of making such void structures. However, "even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production." *In re Thorpe*, 777 F. 2.d 695, 698 (Fed. Cir. 1985) (citations omitted). Appellants do not argue directly that void shapes, sizes, and/or locations otherwise meeting the claimed "arrangement" do not exist in the prior art. We find such an arrangement does exist in the prior art structure of Aoi, and therefore, Appellants' product-by-process limitation of defining such a preexisting product does not define the claimed invention over the prior art.

Accordingly, we have no basis upon which to find error in the Examiner's position. As such, we will sustain the anticipatory rejection of claims 1 and 13 under Aoi, and also the rejection of dependent claims 2-6, 8, 12, and 14 not separately argued.

Anticipation rejection based upon Nishiwaki

Regarding the anticipatory rejection of claims 1, 6, and 7 under Nishiwaki, Appellants similarly dispute the Examiner's finding that Nishiwaki discloses "a precisely-determined arrangement of at least one void formed within the solid structure" as recited in claim 1 (*See App. Br. 7*). As Appellants note, Nishiwaki teaches voids in a gel (*id.*, FF 4). The Examiner cited such voids as meeting the claim (*see Ans. 5*, citing col. 3, l. 61). While the Examiner also cited PZT layers and crystals (*Ans. 5*), in accordance with Appellants' argument (*Reply Br. 4*), we have no basis for finding that such PZT layers and crystals comprise voids as claimed.

As such, we are left with ascertaining whether or not the amorphous gel supports the Examiner's finding that the voids are precisely determined. Following the Examiner's reasoning noted *supra* that a fixed "static" solid precisely defines the void arrangement, because once formed, the voids do not move, we find that Nishiwaki fails to meet the claim. In other words, in our view, because an amorphous gel moves, it follows that the voids therein would not be fixed. As such, the Examiner has failed to make a *prima facie* case of anticipation of claim 1 under Nishiwaki.

Accordingly, we will not sustain the Examiner's anticipatory rejection under Nishiwaki of claim 1, and claims 6 and 7 dependent therefrom.

Anticipation rejection based upon Moslehi

Regarding the anticipatory rejection under Moslehi of claims 1 and 9-11, Appellants similarly dispute the Examiner's finding that Moslehi discloses "a precisely-determined arrangement of at least one void formed within the solid structure" as recited in claim 1. (*See App. Br. 7-8*). Here,

the dispute focuses on whether Moslehi's voids are "formed within a solid structure" (App. Br. 7).

The Examiner finds, and we concur, that Moslehi's windows (squares, rectangles, circles) as depicted at Figures 9-12 constitute voids within the structure (Ans. 5-6, *see* FF 5). Appellants assert that the etched windows "are not voids within the solid structure, but rather 'windows or openings' (see col. 12, line 53) used to provide free flow." (Reply Br. 5). Such an assertion does not explain why such windows are not within the solid structure, and accordingly, does not amount to a demonstration of error in the Examiner's determination. We find that voids defined by such windows are not outside of the structure; hence, they are within the structure, regardless of whether or not they are completely enclosed on all sides by the structure.

Appellants also assert that the mere presence of the windows/voids does not lower the effective dielectric constant of the insulator structure because no metal layers are disclosed. (Reply Br. 5). Such an argument lacks evidentiary support and amounts to an attempt to refute a well known scientific principal that dielectric constants are defined by insulators, not metal layers. As the Examiner generally found, it is well known that voids in insulators inherently decrease such dielectric constants (Ans. 9). We also note that Appellants' claim 1 does not require such metal layers.

Accordingly, we have no basis upon which to find error in the Examiner's position. As such, we will sustain the anticipatory rejections under Moslehi of claim 1 and claims 9-11 not separately argued.

Obviousness rejection based upon Aoi

We also will sustain the obviousness rejection of claims 15 and 16 over Aoi. Appellants rely on their arguments for claim 1, and also assert that the Examiner's "rationale 'since the dielectric constant ultimately affects the RC time delay' does not provide a clear line of reasoning indicating why it would have been obvious to select void diameters of approximately 1 micron or approximately 0.2 micron." (App. Br. 9).

We disagree with Appellants' premise, and consequently, their conclusion. The Examiner also submitted that "Aoi teaches that it is well known that the void diameter is a variable subject to optimization depending on the desired dielectric constant (column 2, lines 8-14 and column 3, lines 11-19)" (Office Action 7, mailed November 4, 2005). The Examiner concluded: "Therefore, it would have been obvious to one of ordinary skill in the art to use a void diameter of either approximately 1 micron or approximately 0.2 micron for the purpose of achieving a desired dielectric constant, since the dielectric constant ultimately affects the RC time delay (column 1, lines 8-16)." (*Id.*)

Appellants have not challenged the Examiner's factual findings. We generally agree with such findings (*see* FF 1-3). Accordingly, we determine that the Examiner has established a *prima facie* case of obviousness which Appellants have not rebutted. Further, we note that "the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR* at 1741 (*quoting In re Kahn*, at 987). Given Aoi's teachings of a specific relationship between void size and dielectric constant, and the level of skill

in the semiconductor arts, in conjunction with the absence of argument/evidence to the contrary, we find that an ordinarily skilled artisan would have predictably altered the molecularly sized voids of Aoi to about 0.2 um and 1.0 um to beneficially adjust the dielectric constant as desired. As such, Appellants have not convinced us of error in the Examiner's ultimate determination of obviousness. *See in re Oetiker*, 977 F.2d 1443, 1445 (Fed. Circ. 1992).

We also find that Appellants disclose as prior art a patent to Farrar (Spec. 17).² Farrar discloses that such void diameters, albeit in polymeric cells, are known. *See* Farrar col. 2, ll. 50-55 – disclosing a “cell size of less than about 3.0 microns, a cell size of less than about 1.0 micron, and even a maximum cell size of less than about 0.1 micron.” Farrar teaches such size provides a low dielectric constant and minimizes capacitive coupling in circuit boards (col. 2, ll. 32-37), and further minimizes the dielectric layer size “to meet the demand for high density ICs” (col. 8, l. 55, generally col. 8, ll. 39-62). Farrar's teaching provides further a motivation for modifying the cell size.

Moreover, a patentability argument directed to a claim feature which is acknowledged to be known in the prior art cannot defeat an obviousness rejection. *In re Reuning*, 2008 WL 1836711, at *3 (Fed. Cir. 2008). *See also Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1570 (Fed. Cir. 1988) (applicant's statement that something is prior art is binding on applicant for determinations of anticipation and obviousness.); *In re Nomiya*,

² Farrar lists Micron Technology, Inc. as the assignee (see cover page [73]), the same assignee, and real party in interest, as involved in this appeal (see App. Br. 2).

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509 F.2d 566, 577 n. 5 (CCPA 1975) (applicant's statement that certain matter is prior art is an admission that the matter is prior art for all purposes). Such an argument is contradicted and therefore vitiated by Appellants' own admission even though the Examiner has not used the admission as evidence in rejecting the claimed invention.

SUMMARY

We sustain the Examiner's rejections of claims 1-6, 8 and 12-14 as being anticipated by Aoi, of claims 1 and 9-11 as being anticipated by Moslehi, and of claims 15 and 16 as being obvious over Aoi. However we do not sustain the Examiner's rejection of claims 1, 6 and 7 as being anticipated by Nishiwaki.

DECISION

We affirm the Examiner's decision rejecting claims 1-6 and 8-16. We reverse the Examiner's decision rejecting claim 7.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a) (1) (iv) (2006).

AFFIRMED-IN-PART

KIS

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

Notice of References Cited	Application/Control No. 10/931,593	Applicant(s)/Patent Under Reexamination	
	Examiner Leonardo Andujar	Art Unit 2800	Page 1 of 1

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*		Document Number	Date	Name	Classification	
		Country Code-Number-Kind Code	MM-YYYY			
	A	US-6,077,792	06-2000		--	--
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



US006077792A

United States Patent [19]

[11] **Patent Number:** **6,077,792**

Farrar

[45] **Date of Patent:** **Jun. 20, 2000**

[54] **METHOD OF FORMING FOAMED POLYMERIC MATERIAL FOR AN INTEGRATED CIRCUIT**

5,879,794 3/1995 Korleski, Jr. .

FOREIGN PATENT DOCUMENTS

000578856 1/1994 European Pat. Off. .
002158995 11/1985 United Kingdom .

[75] Inventor: **Paul A. Farrar**, South Burlington, Vt.

OTHER PUBLICATIONS

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

Jayaraj, K. et al., "Low Dielectric Constant Microcellular Foams", Proceedings from the 7th Meeting of the DuPont Symposium, Wilmington DE. p. 474-501 (1996), Sep. 1996. "Electronic Materials Handbook, vol. 1 Packaging," ASM International, Materials Park OH. p. 105, 767-772 (1989).

[21] Appl. No.: **08/892,114**

Primary Examiner—Charles Bowers
Assistant Examiner—Evan Pert
Attorney, Agent, or Firm—Mueting, Raasch & Gebhardt, P.A.

[22] Filed: **Jul. 14, 1997**

[51] **Int. Cl.**⁷ **H01L 21/469**

[52] **U.S. Cl.** **438/780**; 438/781; 257/759

[58] **Field of Search** 438/780, 781,
438/782; 156/155, 327; 428/209; 257/758,
759, 760

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[57] **ABSTRACT**

A method of forming an insulating material for use in an integrated circuit includes providing a substrate of the integrated circuit and forming a polymeric material on the substrate. At least a portion of the polymeric material is converted to a foamed polymeric material. The converting of the polymeric material includes exposing at least a portion of the polymeric material to a supercritical fluid. Further, an integrated circuit includes a substrate of the integrated circuit and a foamed polymeric material on at least a portion of the substrate. The integrated circuit may further include a conductive layer adjacent the foamed polymeric material. The conductive layer may be a metal line on the foamed polymeric material, or the conductive layer may be an interconnect, e.g., a contact or a via, adjacent the foamed polymeric material.

32 Claims, 8 Drawing Sheets

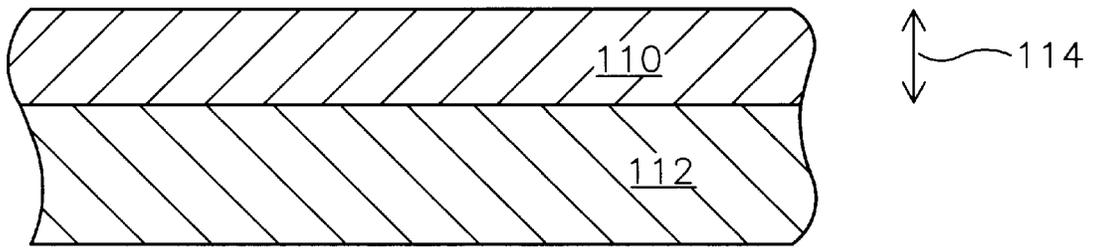


FIG. 1A

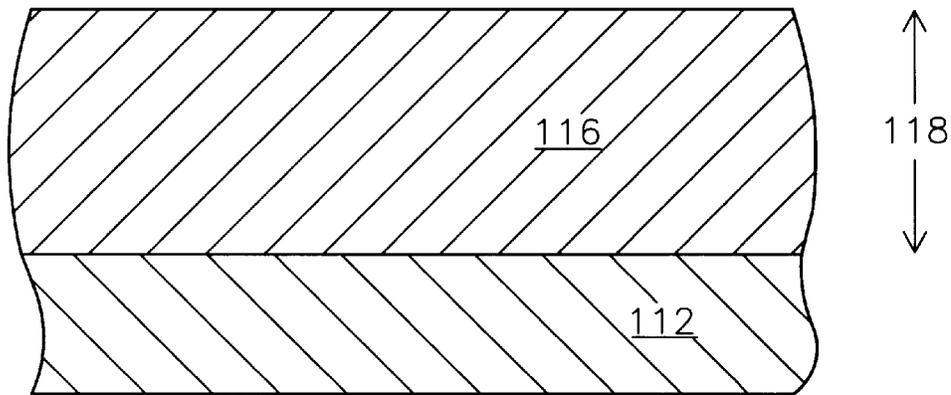


FIG. 1B

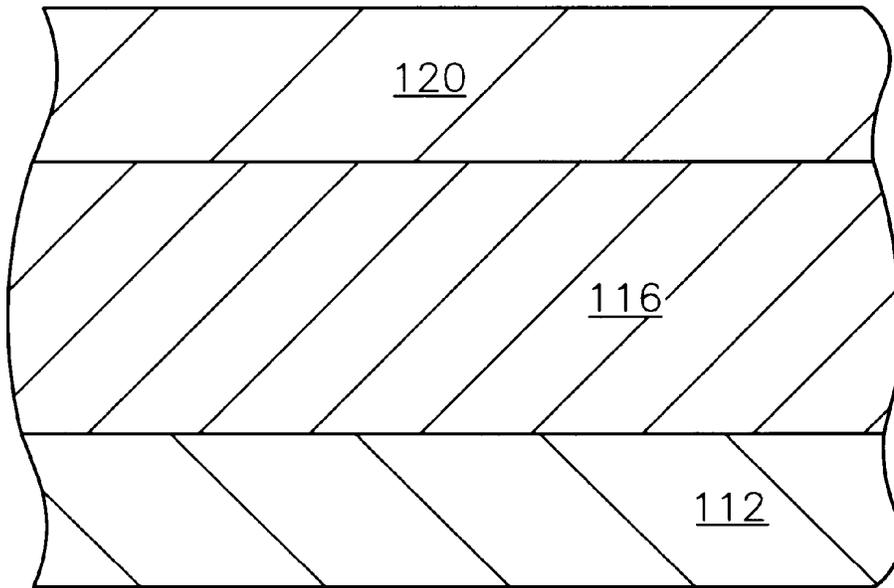


FIG. 1C

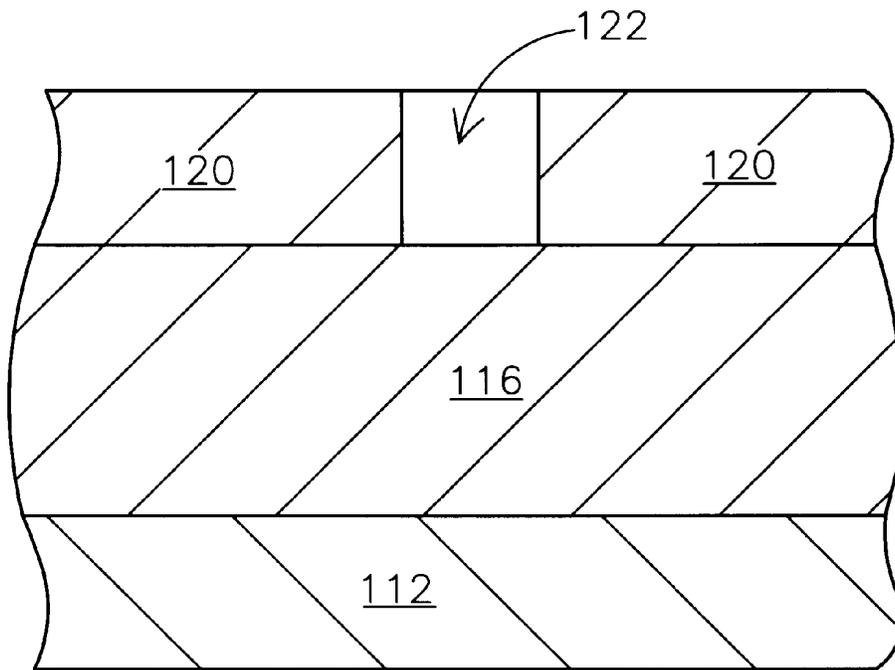


FIG. 1D

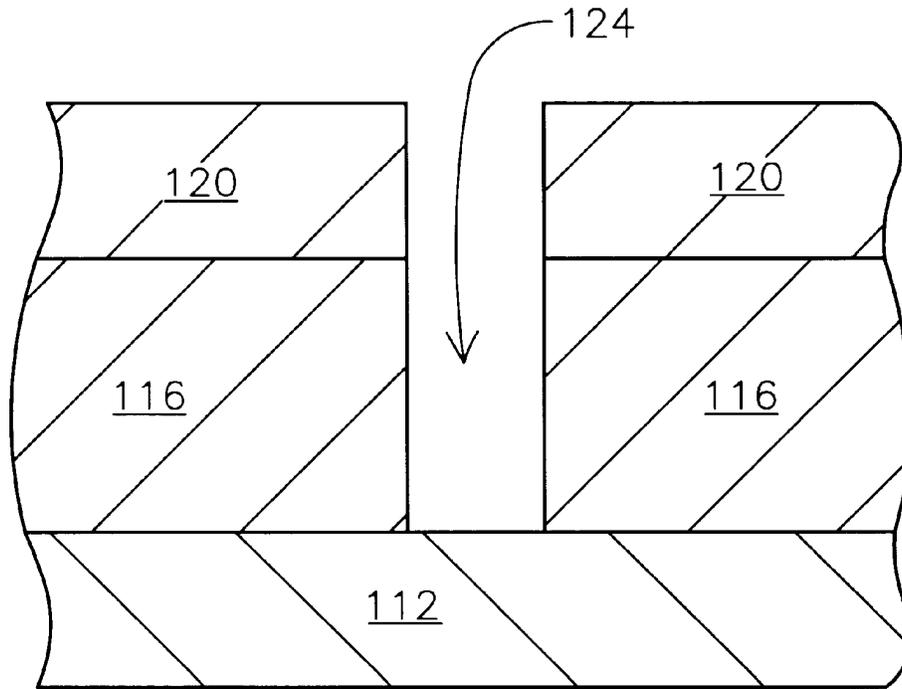


FIG. 1E

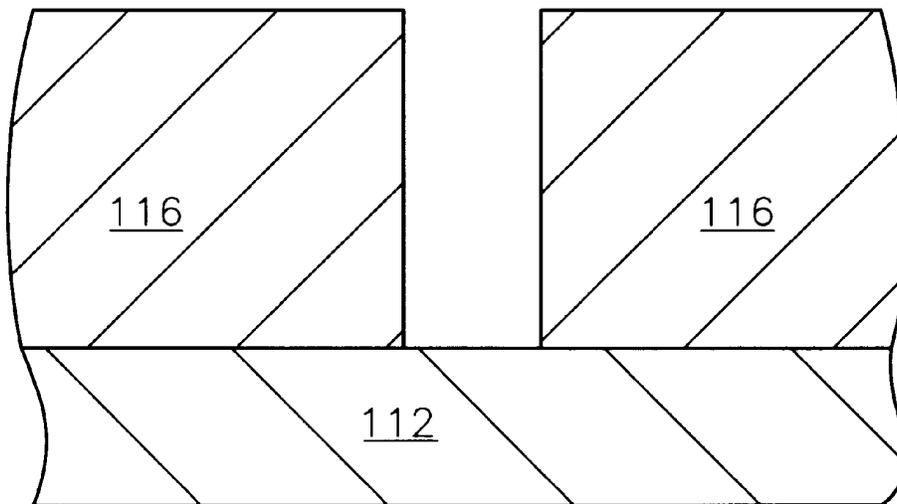


FIG. 1F

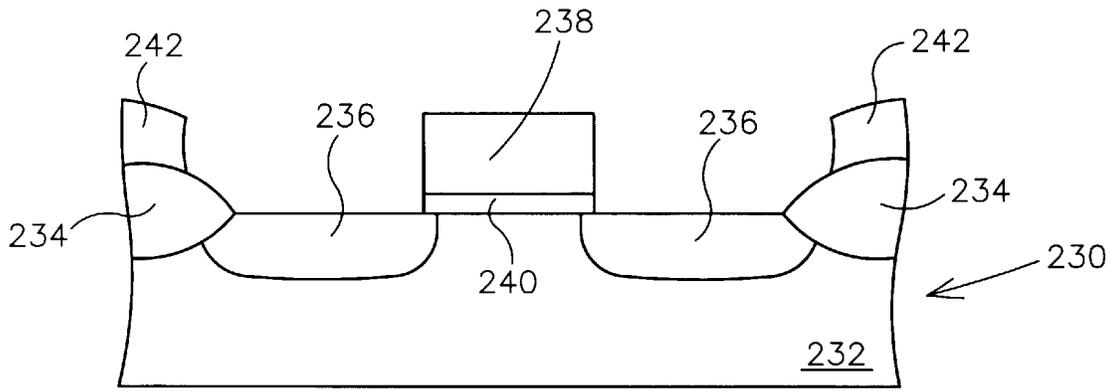


FIG. 2A

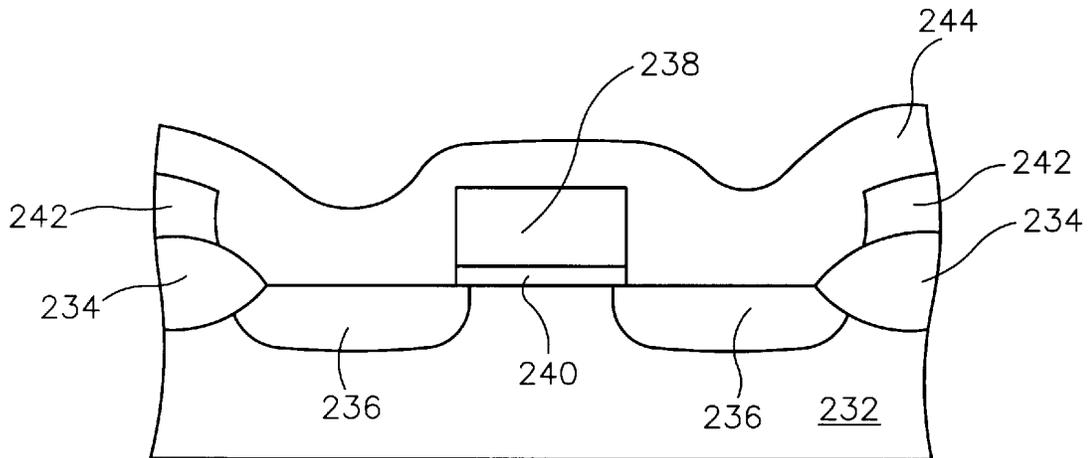


FIG. 2B

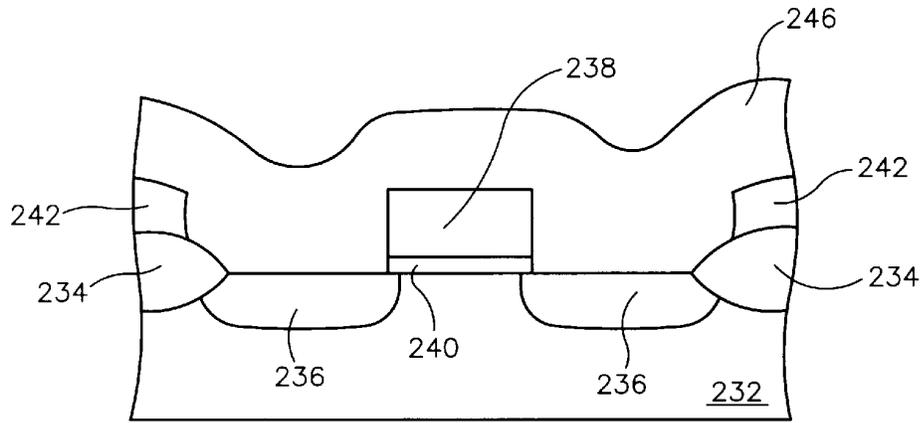


FIG. 2C

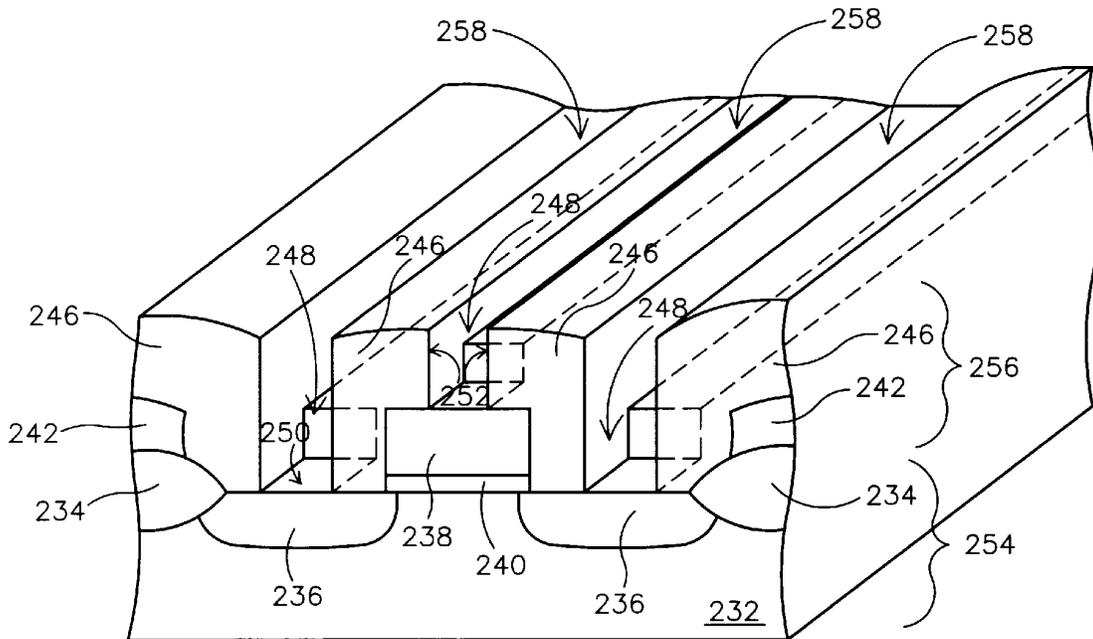


FIG. 2D

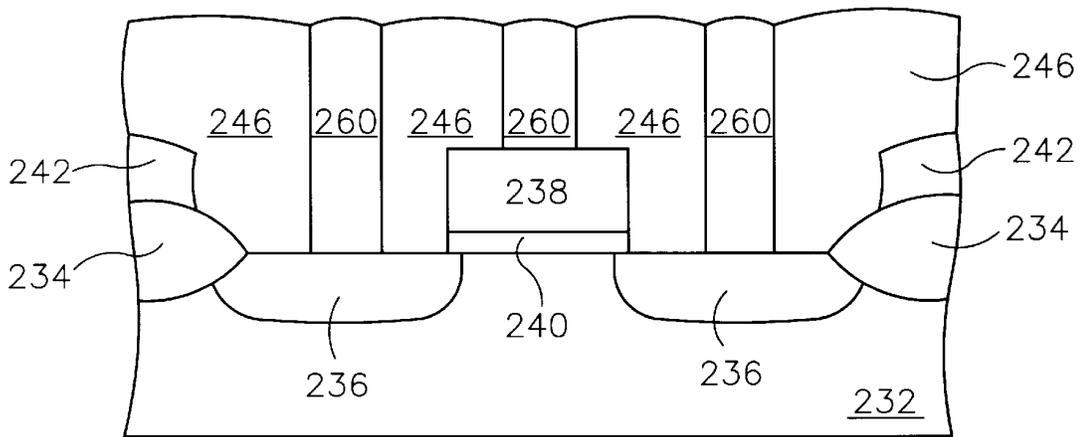


FIG. 2E

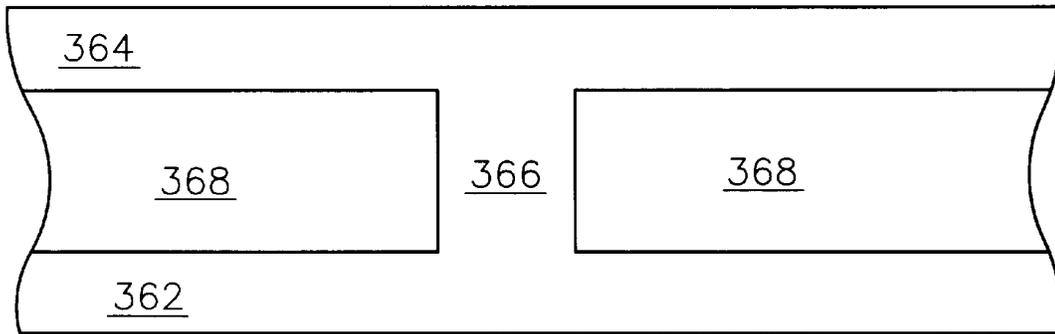


FIG. 3

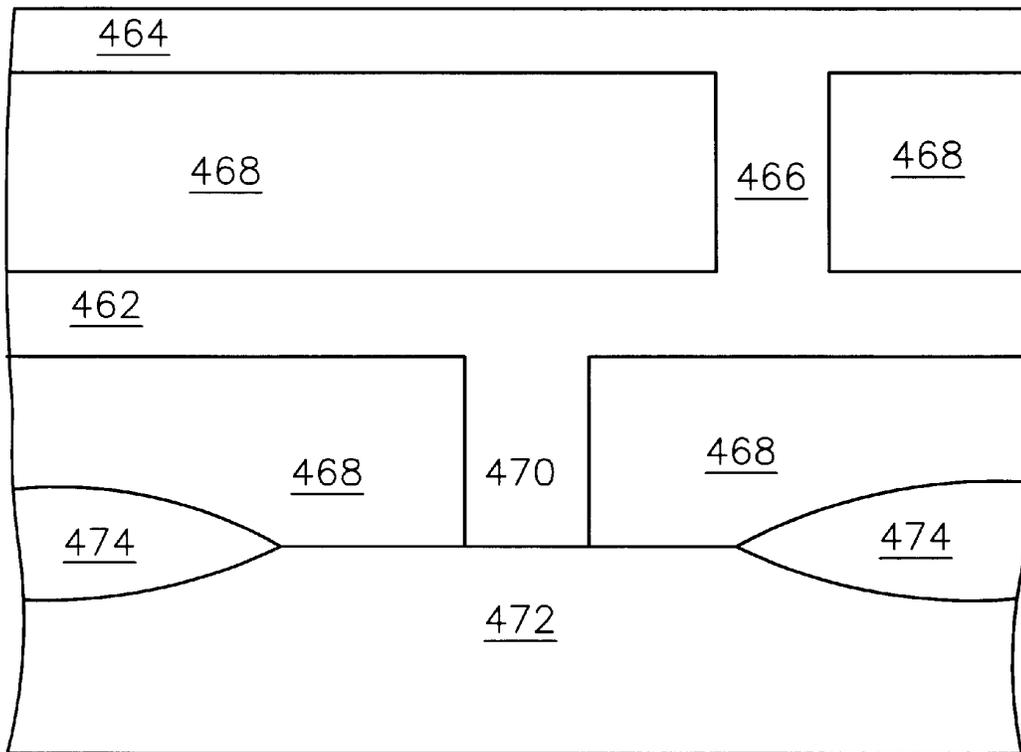


FIG. 4

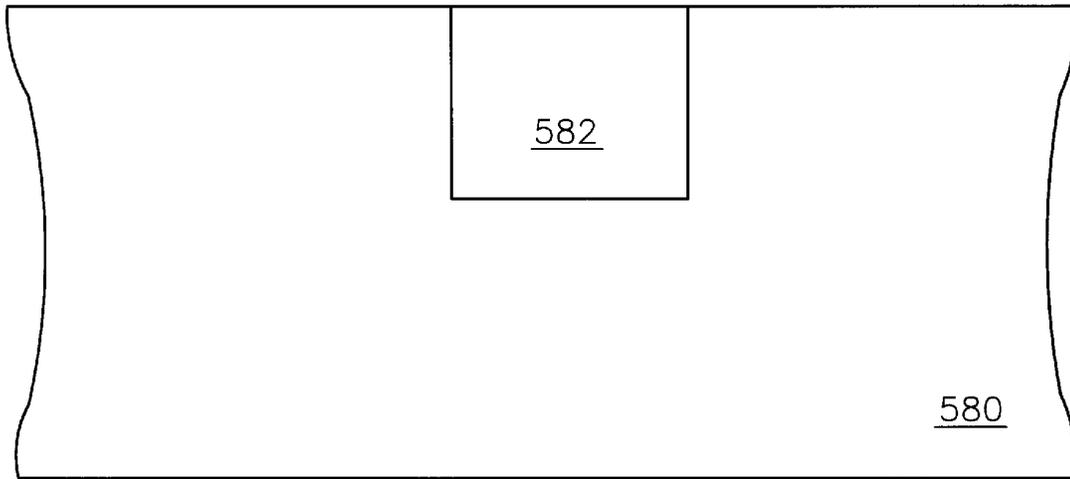


FIG. 5

METHOD OF FORMING FOAMED POLYMERIC MATERIAL FOR AN INTEGRATED CIRCUIT

FIELD OF THE INVENTION

The present invention relates to the fabrication of integrated circuits. More particularly, the present invention relates to insulation materials of an integrated circuit.

BACKGROUND OF THE INVENTION

To meet demands for faster processors and higher capacity memories, integrated circuit (IC) designers are focusing on decreasing the minimum feature size within ICs. By minimizing the feature size within an IC, device density on an individual chip increases exponentially, as desired, enabling designers to meet the demands imposed on them. As the minimum feature size in semiconductor ICs decreases, however, capacitive coupling between adjacent conductive layers is becoming problematic. In particular, for example, capacitive coupling between metal lines in the metallization level of ICs limits the minimum feature size that is operatively achievable.

One attempt to minimize the problem of capacitive coupling between metal lines involves utilizing a relatively low dielectric constant material to insulate the metal lines. Conventionally, silicon dioxide (SiO_2), having a dielectric constant of about $4.0\epsilon_0$ (wherein ϵ_0 is the permittivity of space), is used as the insulating material in ICs. To date, the minimum dielectric constant possible, however, is that of air, the dielectric constant being $1.0\epsilon_0$. Nevertheless, the use of air as an insulating material, such as provided using an air bridge, has drawbacks. For example, IC structures utilizing air insulation lack mechanical strength and protection from their environment.

SiO_2 and air have been utilized together in an inorganic, porous silica xerogel film in order to incorporate both the mechanical strength of SiO_2 and the low dielectric constant of air. In this manner, SiO_2 behaves as a matrix for porous structures containing air. However, porous silica xerogel film has a tendency to absorb water during processing. The water absorbed during processing is released during aging, resulting in cracking and a pulling away of the porous silica xerogel film from the substrate on which it is applied.

Even when nonporous SiO_2 is utilized, as the minimum feature size within an IC decreases, significant stress develops at the interface between the SiO_2 and metal on which SiO_2 is commonly formed, causing potentially detrimental disruptions in the electrical performance of the IC. For example, the stress may be great enough to rupture a metal line adjacent to the SiO_2 insulating layer. Such stress develops from the large difference in the coefficient of thermal expansion between that of SiO_2 and that of the metal. The coefficient of thermal expansion of SiO_2 is about $0.5 \mu\text{m}/\text{m}^\circ\text{C}$. to about $3.0 \mu\text{m}/\text{m}^\circ\text{C}$. The coefficient of thermal expansion of Type 295.0 aluminum, an alloy similar in composition to the aluminum alloys commonly used in the metallization level of an IC, is about $23 \mu\text{m}/\text{m}^\circ\text{C}$. The coefficient of thermal expansion for aluminum is significantly higher than that of SiO_2 . Likewise, the coefficient of thermal expansion of Type C81100 copper, an alloy similar in composition to a copper alloy which may also be used in integrated circuit metallization layers, is about $16.9 \mu\text{m}/\text{m}^\circ\text{C}$., also significantly higher than that of SiO_2 . The metallization layer's larger coefficient of thermal expansion results in its absorption of all of the strain caused by the large difference in the coefficients of thermal expansion upon

heating and cooling. The result of such strain absorption is that the metallization layer is placed in tension and the SiO_2 layer is placed under slight compression. The high compressive yield strength of SiO_2 prevents its rupture. In contrast, the relatively low tensile yield strength of the metallization layer promotes its rupture, leading to integrated circuit failure.

It has also been reported that certain polymeric materials have dielectric constants less than that of SiO_2 . For example, polyimides are known to have a dielectric constant of about $2.8\epsilon_0$ to about $3.5\epsilon_0$. The use of polyimides in the metallization level of ICs is well known. For example, Carey (U.S. Pat. No. 5,173,442) reported the use of a polyimide as an interlayer dielectric.

Others have reported that foaming (i.e., introducing air into) polymeric material results in a material having a dielectric constant of about $1.2\epsilon_0$ to about $1.8\epsilon_0$. One such foaming process is described by Cha et al. (U.S. Pat. No. 5,158,986). The exact dielectric constant of such foamed polymers depends on the percentage of voids (i.e., air) present and the dielectric constant of the polymeric material that was foamed. The use of such foamed polymers, however, has been limited to electronic packaging applications and multichip module applications for microwave substrates. Multichip module processing is not suitable for use in semiconductor fabrication because in multichip module processing, a metal insulator "sandwich" is formed as a unit and is then applied to a surface. Due to the oftentimes uneven topographies at the metallization level of an IC, each of the metal layer and the insulation layer need to be formed separately, allowing them to conform to the underlying topography.

Therefore, there is a need for an insulating material for use in an integrated circuit that has adequate mechanical integrity, as well as a relatively low dielectric constant. The capacitive coupling problem between conductive layers needs to be minimized as device density continues to increase within an integrated circuit.

SUMMARY OF THE INVENTION

A method of forming an insulating material for use in an integrated circuit in accordance with the present invention includes providing a substrate of the integrated circuit and forming a polymeric material on the substrate. At least a portion of the polymeric material is converted to a foamed polymeric material.

The step of converting the polymeric material comprises exposing at least a portion of the polymeric material to a supercritical fluid. Preferably, the supercritical fluid is carbon dioxide.

In another embodiment of the method, the step of converting the polymeric material includes converting at least a portion of the polymeric material to a foamed polymeric material having a maximum cell size of less than about 3.0 microns, a cell size of less than about 1.0 micron, and even a maximum cell size of less than about 0.1 micron.

Further, a method of fabricating an interconnect for an integrated circuit in accordance with the present invention is described. The method includes providing a substrate that includes an active area of the integrated circuit and forming a polymeric material on the substrate. At least a portion of the polymeric material is converted to a foamed polymeric material and at least one contact hole is defined in the foamed polymeric material to the active area of the integrated circuit. The contact hole is then filled with a conductive material. In much the same manner, a method of fabricating a via in the foamed polymeric material is described.

In such various methods, the polymeric material on the substrate may be an organic polymer, an organic oligomer, and an organic monomer. Preferably, the polymeric material on the substrate is an organic polymer selected from the group of a polyimide, a fluorinated polymer, and a parylene. More preferably, the polymeric material selected from the group of Type I polyimide, Type III polyimide, and Type V polyimide, or the polymeric material is a fluorinated polyimide. Most preferably, the polymeric material includes a Type I polyimide or a fluorinated Type I polyimide.

Further in accordance with the present invention, an integrated circuit is described which includes a substrate of the integrated circuit and a foamed polymeric material on at least a portion of the substrate. In various embodiments, the integrated circuit further includes a conductive layer adjacent the foamed polymeric material. The conductive layer may be a metal line on the foamed polymeric material, or the conductive layer may be an interconnect, e.g., a contact or a via, adjacent the foamed polymeric material.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1A is a cross-sectional representation of a substrate having polymeric material thereon.

FIG. 1B is a cross-sectional representation of the substrate of FIG. 1A, wherein the polymeric material of FIG. 1A has been converted to foamed polymeric material.

FIGS. 1C through 1F are cross-sectional representations of intermediate and resulting structures, wherein the foamed polymeric material of FIG. 1B is optionally patterned.

FIG. 2A is a cross-sectional representation of a substrate.

FIG. 2B is a cross-sectional representation of the substrate of FIG. 2A, wherein a polymeric material is formed thereon.

FIG. 2C is a cross-sectional representation of the structure of FIG. 2B, wherein the polymeric material is foamed.

FIG. 2D is a perspective cross-sectional representation of the structure of FIG. 2C, wherein contact holes and trenches are defined in the foamed polymeric material.

FIG. 2E is a cross-sectional representation of the structure of FIG. 2D, wherein the contact holes and trenches are filled with metal to form the metallization level of the substrate.

FIG. 3 is a cross-sectional representation of a metallization level of an integrated circuit utilizing foamed insulating material in accordance with the present invention.

FIG. 4 is a cross-sectional representation of another embodiment of a metallization level of an integrated circuit utilizing foamed insulating material in accordance with the present invention.

FIG. 5 is a cross-sectional representation of trench isolation utilizing foamed insulating material in accordance with the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

In accordance with the present invention, foamed polymeric material is utilized as an insulating material within an integrated circuit (IC). Polymeric materials are meant to include organic polymers (i.e., materials containing 5 or more mer units having carbon chain backbones), organic oligomers (i.e., materials containing 2 to 4 mer units having carbon chain backbones), organic monomers (i.e., materials containing one mer unit having a carbon chain backbone), and materials having properties similar to those of organic polymers. For example, organic polymers are often charac-

terized by having at least one of high ductility, a low elastic modulus (also referred to as Young's Modulus (E)), a low compressive yield strength, and a low coefficient of thermal expansion. In comparison, polymeric materials, as referred to herein, do not include brittle materials, such as ceramics, that are often characterized by their high compressive yield strength. Furthermore, polymeric materials will exhibit a tendency to flow more readily, making their application much easier than, for example, ceramic materials. Any of the above polymeric materials capable of being foamed, however, is suitable for use in accordance with the present invention.

The use of foamed polymeric material advantageously provides a lower dielectric constant insulating material within an IC relative to conventional silicon dioxide (SiO₂). Foamed polymeric material combines the minimal dielectric constant of air, 1.0ε₀, with the mechanical strength of the polymeric material. The polymeric material behaves as a matrix for porous structures containing air. The lower dielectric constant of such foamed polymeric material allows its advantageous use in ICs where capacitive coupling has typically been problematic. Foamed polymeric material provides relief for capacitive coupling problems.

Foamed polymeric material has many advantages. For example, unlike conventional SiO₂, which has a dielectric constant of about 4.0ε₀ and is used as the matrix in porous silica xerogel films, the polymeric matrix materials utilized in the porous insulating material of the present invention can have lower dielectric constants relative to that of SiO₂. Thus, the resulting foamed polymeric material can have a potentially lower dielectric constant than that of a porous silica xerogel film, depending on the percentage of voids within the material and the dielectric constant of the polymeric matrix material.

Furthermore, for example, foamed polymeric materials are advantageously more ductile than many other materials, such as porous silica xerogel films. The potential ductility of foamed polymeric material is due to the polymeric matrix. The polymeric matrix can be selected such that it has a high ductility. Ceramic matrix materials, such as SiO₂ used in porous silica xerogel film, are characterized by their lack of ductility. Foamed polymeric materials have a lesser tendency to crack and pull away from the substrate on which they are applied than do the counterpart porous silica xerogel films.

Foamed polymeric material of the present invention is advantageously utilized to insulate conductive layers, such as metal lines, within an IC. Depending on the temperatures to which the foamed polymeric material will be subjected after its formation, the foamed polymeric material can be utilized anywhere an insulating material is needed within an IC. For example, the foamed polymeric material can be utilized as a device level insulating material, as long as subsequent processing temperatures do not exceed the temperature at which the foamed polymeric material becomes unstable. At this time, processing temperatures at the device level are typically as high as about 800° C. to about 1,100° C., particularly during deposition and annealing process steps. Many conventional polymeric materials are not stable at such high temperatures. With the rapid evolution of high density IC processing, however, the use of foamed polymeric materials at the device level according to the present invention may soon be readily apparent.

In comparison, use of foamed polymeric materials as a metallization level insulating material generally assures that the material will not be subjected to high processing tem-

peratures. At the metallization stage in the fabrication process, most of the high temperature steps have already occurred. Thus, many foamed polymeric materials are suitable for use in the metallization level because they can withstand the relatively low subsequent processing temperatures as compared to when the foamed polymeric material is used on the device level. On the device level, the foamed polymeric material may be subjected to high subsequent processing temperatures.

For the reasons stated above, preferably, the polymeric material utilized is able to withstand high subsequent processing temperatures in order to maximize the locations in which it can be utilized in an IC. Thus, preferred polymeric materials include polyimides due to their relative stability at higher temperatures. Some polyimides are able to withstand exposure to temperatures as high as 232° C. for extended periods of time. Other polyimides are able to withstand exposure to temperatures as high as 316° C. for extended periods of time. Type III polyimides have a decomposition temperature of 580° C. and a glass transition temperature above 320° C. Type I and Type V polyimides, have decomposition temperatures of 580° C. and 620° C., respectively. These materials both have glass transition temperatures above 400° C. Such characteristics are found in "The Electronic Materials Handbook—Volume 1 Packaging," ASM International, Metals Park, Ohio (1989). Polyimides may also be able to withstand exposure to higher temperatures for shorter durations. Both Type I and Type V polyimides can be exposed to temperatures up to 450° C. for about one to two hours without significant weight loss, although some out gassing may occur between 430° C. and 450° C.

There are a wide variety of suitable polyimides available. Polyimides are usually prepared by reacting a dianhydride and an aromatic diamine. The resulting polyimide is classified according to the type of dianhydride used. For example, Type I, Type III, and Type V polyimides are readily available and suitable for use in accordance with the present invention. Type I polyimide is prepared from pyromellitic dianhydride (PMDA) and oxydianiline (ODA). Type III polyimide is prepared from 4-4'-benzophenone dicarboxylic dianhydride (BTDA). Type V polyimide is prepared from biphenyl dianhydride (BPDA).

Type I polyimide has an elastic modulus of about 1.4 GPa and a coefficient of thermal expansion of about 20 $\mu\text{m}/\text{m}^\circ\text{C}$. Type III polyimide has an elastic modulus of about 2.4 GPa and a coefficient of thermal expansion of about 40 $\mu\text{m}/\text{m}^\circ\text{C}$. Type V polyimide has an elastic modulus of about 8.3 GPa and a coefficient of thermal expansion of about 40 $\mu\text{m}/\text{m}^\circ\text{C}$.

Preferably, a Type I polyimide is utilized due to its relatively high ductility and relatively low coefficient of thermal expansion. Type 295.0 aluminum has an elastic modulus of about 70 GPa and a coefficient of thermal expansion of about 23 $\mu\text{m}/\text{m}^\circ\text{C}$. Type C81100 copper has an elastic modulus of about 115 GPa and a coefficient of thermal expansion of about 16.9 $\mu\text{m}/\text{m}^\circ\text{C}$. Thus, due to the similarities in the coefficients of thermal expansion between the Type I polyimide and the metallization layer, thermally induced stress is minimized. Furthermore, the high ductility of Type I polyimide, as shown by its low elastic modulus (about 1.4 GPa), allows it to absorb any thermally induced stress that may occur. When such polymeric material is foamed, the elastic modulus should be reduced, while the coefficient of thermal expansion should remain about the same as that of the unfoamed polymeric material.

Other suitable polymeric materials include, for example, parylene and fluorinated polymers. Parylene-N has a melting

point of 420° C., a tensile modulus of 2.4 GPa, and a yield strength of 42 MPa. Parylene is based on p-xylylene and is prepared by vapor-phase polymerization.

The use of fluorinated polymers, preferably fluorinated polyimides, and more preferably fluorinated Type I polyimides have certain advantages. It is well known that the fluorine containing polymers have lower dielectric constants than similar polymers without fluorine additions. An additional advantage of the fluorine containing polymers is based on such polymers tending to be hydrophobic by nature. Such a tendency insures that even if water diffuses through the foamed polymer it will not condense in the voids so as to increase the dielectric constant of the foamed material.

FIGS. 1A to 1C illustrate general process steps utilized to form a foamed polymeric material on a substrate. First, the substrate can optionally be placed in a low temperature furnace for a dehydration bake (e.g., about 30 minutes at about 150° C.) in order to remove residual moisture on the surface of the substrate.

In order to form a foamed polymeric insulation layer in an IC, a polymeric material **110** is applied to the substrate **112**, as illustrated in FIG. 1A. The term substrate, as used herein, refers to any semiconductor-based structure. Substrate includes silicon wafers, silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor, as well as other semiconductor-based structures well known to one skilled in the art. Furthermore, when reference is made to a substrate in the following description, previous process steps may have been utilized to form regions/junctions in the semiconductor-based structure previously formed. The process steps may have been used to form any number of layers or other material structures. In one embodiment of the invention, the substrate will include a metallization layer, such as aluminum or an aluminum alloy (e.g., aluminum alloyed with copper and/or silicon).

A wide variety of methods are available for applying the polymeric material **110** to the substrate **112**. For example, spin-on coating, spraying, and dipping may be utilized to apply polymers to the substrate **112**. Furthermore, a combination of such application techniques or any other techniques known to one skilled in the art may be used. The thickness of the layer of polymeric material **110**, as indicated by arrow **114**, is adjusted according to the desired thickness of the resulting foamed polymeric material, taking into account the foam expansion rate of the foaming process utilized. For example, the thickness of the layer of polymeric material may be in the range of about 0.1 microns to about 1.0 microns. The thickness of the resulting foamed polymeric material should be such that it provides adequate electrical insulation without preventing a decrease in the minimum achievable feature size of the IC. For many applications, a foamed polymeric material thickness of about 0.7 micron to about 2.1 microns is sufficient to provide adequate electrical insulation. Foamed polymer thicknesses above 2.1 microns may be desirable where metal thicknesses above 2.0 microns are used. Such foamed polymeric thicknesses may range from about 0.2 microns up to about 10.0 microns or even more. Depending on the application, however, the thickness of the polymeric material **110** is adjusted according to these criteria and known methods for controlling the thickness of applied polymeric material **110** using those techniques. For example, when utilizing spin-on coating, the thickness can be varied by adjusting the rotational speed and/or the acceleration of the spinner.

After the polymeric material **110** is applied to the substrate **112**, an optional low temperature bake can be done to

drive off most of the solvents present in the polyimide. Next, the polymeric material **110** is cured, if needed. In the case of an organic polymer, cured typically means that the polymeric material develops a large number of cross-links between polymer chains. Techniques for curing polymers are well known to one skilled in the art and any number of curing methods may be suitable for the processing described herein. For example, many conventional polymers can be cured by baking them in a furnace (e.g., about a 350° C. to about a 500° C. furnace) or heating them on a hot plate. Other conventional polymers can be cured by exposing them to visible or ultraviolet light. Still other conventional polymers can be cured by adding curing (e.g., cross-linking) agents to the polymer. It is preferred, when using Type I polymers, to use a multiple step cure to achieve maximum effectiveness. For example, such a multiple step cure may include processing in the range of about 100° C. to about 125° C. for about 10 minutes, about 250° C. for about 10 minutes, followed by about 375° C. for about 20 minutes. It should be readily apparent to one skilled in the art that the times and temperatures may vary depending upon various factors, including the desired properties of the materials used, and that the present invention is in no manner limited to the illustrative multiple step cure presented above. Various multiple step curing methods may be suitable. Preferably, hot plate curing is used.

A supercritical fluid is then utilized to convert at least a portion of the polymeric material **110**, as illustrated in FIG. 1A, into a foamed polymeric material **116** having a thickness **118**, as illustrated in FIG. 1B. A gas is determined to be in a supercritical state (and is referred to as a supercritical fluid) when it is subjected to a combination of pressure and temperature so that its density approaches that of a liquid (i.e., the liquid and gas state coexist). A wide variety of compounds and elements can be converted to the supercritical state in order to be used to form the foamed polymeric material **116**.

Preferably, the supercritical fluid is selected from the group of ammonia (NH₃), an amine (NR₃), an alcohol (ROH), water (H₂O), carbon dioxide (CO₂), nitrous oxide (N₂O), a noble gas (e.g., He, Ne, Ar), a hydrogen halide (e.g., hydrofluoric acid (HF), hydrochloric acid (HCl), hydrobromic acid (HBr)), boron trichloride (BCl₃), chlorine (Cl₂), fluorine (F₂), oxygen (O₂), nitrogen (N₂), a hydrocarbon (e.g., dimethyl carbonate (CO(OCH₃)₂), methane (CH₄), ethane (C₂H₆), propane (C₃H₈), ethylene (C₂H₄), etc.), a fluorocarbon (e.g., CF₄, C₂F₄, CH₃F, etc.), hexafluoroacetylacetone (C₅H₂F₆O₂), and combinations thereof. Although these and other fluids may be used, it is preferable to have a fluid with a low critical pressure, preferably below about 100 atmospheres, and a low critical temperature of at or near room temperature. Further, it is preferred that the fluids be nontoxic and nonflammable. Likewise, the fluids should not degrade the properties of the polymeric material used. Most preferably, however, the supercritical fluid is CO₂, due to the relatively inert nature of CO₂, with respect to most polymeric materials. Furthermore, the critical temperature (about 31° C.) and critical pressure (about 7.38 MPa, 72.8 atm) of CO₂ are relatively low. Thus, when CO₂ is subjected to a combination of pressure and temperature above about 7.38 MPa (72.8 atm) and about 31° C., respectively, it is in the supercritical state.

The structure illustrated in FIG. 1A, is exposed to the supercritical fluid for a sufficient time period to foam at least a portion of the polymeric material **110** to the desired resulting thickness **118**, as illustrated in FIG. 1B. Generally, the substrate **112** is placed in a processing chamber and the

temperature and pressure of the processing chamber are elevated above the temperature and pressure needed for creating and maintaining the particular supercritical fluid. After the polymeric material **110** is exposed to the supercritical fluid for a sufficient period of time to saturate the polymeric material **110** with supercritical fluid, the flow of supercritical fluid is stopped and the processing chamber is depressurized. Upon depressurization, the foaming of the polymeric material occurs as the supercritical state of the fluid is no longer maintained.

The foaming of a particular polymeric material may be assisted by subjecting the material to thermal treatment, e.g., a temperature suitable for assisting the foaming process but below temperatures which may degrade the material. Further, the depressurization to ambient pressure is carried out at any suitable speed, but the depressurization must at least provide for conversion of the polymeric material before substantial diffusion of the supercritical fluid out of the polymeric material occurs. Foaming of the polymeric material occurs over a short period of time. The period of time that it takes for the saturated polymeric material to be completely foamed depends on the type and thickness of the polymeric material and the temperature/pressure difference between the processing chamber and ambient environment. The specific time, temperature, pressure combination used depends on the diffusion rate of the gas through the polymer and the thickness of the layer of polymer used. It should be readily apparent that other foaming techniques may be used in place of or in combination with that described herein in accordance with the present invention. Foams may also be formed by use of block co-polymers as described in "Low Dielectric Constant Polyimides and Polyimide Nanofoams," by R. D. Miller et al., *Proceedings From the Seventh Meeting of the Dupont Symposium on Polyimides in Microelectronics*, Wilmington, Del., Sep. 16-18, 1996. However, use of such co-polymers have the disadvantage in that the chemical reaction must be initiated and controlled on the surface of the semiconductor wafer.

The foamed polymeric material **116**, as illustrated in FIG. 1B, is readily characterized by the number and size of cells distributed therein. Cell, as used herein, refers to an enclosed region of air. The size of a cell is determined by the nominal diameter of the enclosed region of air. Preferably, the size of cells according to the present invention is no greater than about 3.0 microns. More preferably, the size of cells according to the present invention is less than about 1.0 micron. In some applications, the size of cells according to the present invention is below 0.1 micron. It is desirable to have small cell sizes so that the foamed polymeric material **116** can be utilized in extremely small spaces. For example, as device density increases along with minimization in feature sizes, the space between metal lines in the metallization level is becoming increasingly small. This is the reason that capacitive coupling occurs between such metal lines. In order to meet the demand for high density ICs with minimal feature sizes, it is necessary that foamed polymeric material **116** be able to be formed in such small dimensions. As long as the maximum cell size of the foamed polymeric material is smaller than the minimum distance between metal lines, foamed polymeric materials provide adequate electrical insulation without a potentially detrimental reduction in mechanical integrity.

The foamed polymeric material **116** can be patterned by conventional photolithography and etching processes, if desired. Such optional processing steps are illustrated in FIGS. 1C-1F. First, as illustrated in FIG. 1C, a resist layer **120** (e.g., photoresist) is coated on the foamed polymeric

material **116**, as well known to one skilled in the art. Next, the resist layer **120** is exposed (e.g., utilizing photolithography) and developed, as well known to one skilled in the art, resulting in a patterned layer including resist **120** and throughholes **122** to the underlying foamed polymeric material **116**, as illustrated in FIG. 1D. The foamed polymeric material **116** is then etched using suitable etch chemistries for the type of polymeric material. For example, most organic polymers can be etched using an oxygen plasma. The etched structure is illustrated in FIG. 1E, wherein a throughhole **124** extends through the foamed polymeric material **116** to the underlying substrate **112**. Then, as illustrated in FIG. 1F, the resist layer **120**, illustrated in FIG. 1E, is removed by use of standard photoresist removal methods, such as wet resist stripping agents. Subsequent processing steps, if any, are then performed, as well known to one skilled in the art of semiconductor processing.

A more specific use of the present invention is illustrated by way of FIGS. 2A–2E. FIGS. 2A–2E illustrate the use of dual damascene metallization process with foamed polymeric material as the insulating interlayer dielectric material. Cronin et al. (U.S. Pat. No. 4,962,058) discusses the dual damascene process in more detail than what will be provided herein. The specific use illustrated in FIGS. 2A–2E is the dual damascene metallization of a transistor. The application of the foamed polymeric material of the present invention, however, is not meant to be limited to the dual damascene metallization of transistor devices. Many devices, such as memory cells and capacitors, can be metallized using such a dual damascene process with a foamed polymeric material as the interlayer dielectric.

As illustrated in FIG. 2A, a substrate **230** is conventionally processed up to the point where the first level of interconnection metal is to be formed and will not be described in detail herein. The first level of interconnection metal is typically termed the contact because it connects the first metal line to an active area on an underlying device. In FIG. 2A, the device is a transistor. The transistor is laterally isolated on a doped silicon wafer **232** by field oxide **234**. Implanted source/drain regions **236** are formed in the doped silicon wafer **232** on either side of a gate **238** and gate oxide **240** stack. Patterned polysilicon **242** typically remains on the field oxide **234** from the gate **238** patterning step.

As illustrated in FIG. 2B, a layer of polymeric material **244** is then applied to the substrate **230** illustrated in FIG. 2A. At least a portion of the polymeric material **244** illustrated in FIG. 2B is then converted to a foamed polymeric material **246** as illustrated in FIG. 2C. The technique for converting the polymeric material **244** to a foamed polymeric material **246** was described previously with respect to FIGS. 1A–1B. At this point, the foamed polymeric material may be planarized using known planarization methods, such as using etch back techniques or more preferably chemical mechanical planarization techniques.

As illustrated in FIG. 2D, contact holes **248** are defined to active areas **236** and **238** of the transistor. Optionally, barrier materials, such as titanium nitride or titanium silicide, can be formed on the bottom **250** and/or sidewalls **252** of the contact holes **248**. Techniques for forming such materials are well known to one of ordinary skill in the art. For simplicity, such barrier materials are not illustrated in FIG. 2D. At this point it is convenient to point out the device level **254** of the substrate underlying the metallization level **256** of the substrate. In the metallization level **256** of the substrate, trenches **258** are defined in the foamed polymeric material **246**. Trenches **258** extend over the contact holes **248** and define the position and width of metal lines that are subsequently formed therein.

To form the contact holes **248** and trenches **258**, the structure illustrated in FIG. 2C is patterned using conventional photolithography and etching. Such steps are described previously with respect to FIGS. 1C–1F. Due to the nature of the dual damascene process, the depth of the etch is variable across the surface of the substrate, e.g., the etch depth is greater where contact holes **248** are defined and less where only trenches **258** are defined between devices. Thus, two mask and etch steps can be utilized in a conventional photolithographic process to define the contact holes **248** separately from the trenches **258**. Alternatively, a gray mask pattern can be utilized to define the contact holes **248** and trenches **258** simultaneously in one photolithographic mask and etch step.

Next, as illustrated in FIG. 2E, metal **260** is deposited and etched back in the contact holes **248** and trenches **258**. Typically, the metal **260** is aluminum (Al) or an aluminum alloy. Preferable aluminum alloys include Al/Cu and Al/Cu/Si alloys. A wide variety of suitable methods are available for depositing the metal **260**. Most techniques are physical techniques (e.g., sputtering and evaporating). The advantage of a dual damascene process is that only one metal **260** deposition step is needed to fill both the contact holes **248** and trenches **258**. Excess metal **260** deposited outside of the defined contact holes **248** and trenches **258** is etched back using any suitable method. For example, planarization (e.g., using at least one of a chemical or mechanical technique) is one useful method. The sequence of steps illustrated in FIGS. 2B–2E is then repeated, if necessary, depending on the number of conductive layers in the metallization level of the substrate.

FIG. 3 illustrates, in general, one embodiment of part of a metallization level of an integrated circuit. A first conductive layer **362** (e.g., metal line) is electrically connected to a second conductive layer **364** (e.g., metal line) with a conductive via **366**. Foamed insulating material **368** in accordance with the present invention electrically insulates the first and second conductive layers **362** and **364**. The process utilized to form the structure illustrated in FIG. 3 is readily apparent given the preceding examples. This structure can be formed utilizing dual damascene techniques or standard processing techniques. Details of these processes will not be further recited here.

FIG. 4 illustrates another embodiment of a metallization level of an integrated circuit. A first conductive layer **462** is electrically connected to a second conductive layer **464** with a conductive via **466**. Note that the via **466** is not coincident with the contact **470** to the underlying device. Alternatively, the via **466** can be formed coincidentally with the contact **470** to the underlying device. Foamed insulating material **468** in accordance with the present invention electrically insulates the first and second conductive layers **462** and **464**. Foamed insulating material **468** also electrically insulates the first conductive layer **462** from an active area, represented generally as **472**, of an underlying substrate. Device level insulation **474** can be silicon dioxide or foamed insulating material of the present invention if processing temperatures permit. This structure can be formed utilizing dual damascene techniques or standard processing techniques. Details of these processes will not be further recited here.

FIG. 5 illustrates trench isolation in general and in accordance with the present invention. A trench is etched in a substrate **580** utilizing conventional processing. Foamed insulating material **582** is then formed in the trench etched in the substrate **580**. This process is applicable to both shallow trench isolation and deep trench isolation. Process-

ing times will vary between the two types of trench isolation, however. For deep trench isolation, longer exposure to the supercritical fluid may be necessary to adequately convert substantially all of the polymeric material to the foamed polymeric material. Thus, efficient use of this process may be limited for deep trench isolation, depending on the device density of the integrated circuit in which it is utilized.

All patents disclosed herein are incorporated by reference in their entirety, as if individually incorporated. The foregoing detailed description and examples have been given for clarity of understanding only. No unnecessary limitations are to be understood therefrom. The invention is not limited to the exact details shown and described, as variations obvious to one skilled in the art will be included within the invention defined by the claims. For example, the foamed polymeric material of the present invention can be utilized as an interlayer dielectric insulating material where the metal lines are formed by a variety of methods. This includes single damascene metallization and conventional (i.e., non-damascene) metallization techniques. Furthermore, the foamed polymeric material can be utilized anywhere an electrical insulation material is needed, so long as the polymeric material is stable at the temperatures that it will subsequently be subjected to. For example, the foamed polymeric material can be formed adjacent a conductive layer. A wide variety of other uses are also suitable for use of the present invention. For example, the present invention is also suitable for forming capacitors having a foamed insulating material dielectric layer therein.

It is not necessary that all polymeric insulating material within an integrated circuit by converted to foamed insulating material in accordance with the present invention. It is only necessary to convert a portion of the polymeric material to the foamed polymeric material to obtain the benefits of the present invention. Furthermore, foamed polymeric material of the present invention can be utilized in conjunction with other insulating material. For example, adjacent layers of foamed polymeric material and silicon dioxide insulating material can be utilized in regions of an integrated circuit where different electrical isolation is desired.

What is claimed is:

1. A method of forming an insulating material for use in an integrated circuit, the method comprising the steps of: providing a substrate of the integrated circuit; forming a polymeric material on the substrate; and converting at least a portion of the polymeric material formed on the substrate to a foamed polymeric material, wherein the step of converting the polymeric material comprises exposing at least a portion of the polymeric material to a supercritical fluid.
2. The method of claim 1, wherein the step of forming the polymeric material on the substrate comprises forming a polymeric material selected from the group of an organic polymer, an organic oligomer, and an organic monomer.
3. The method of claim 2, wherein the step of forming the polymeric material on the substrate comprises forming an organic polymer selected from the group of a polyimide, a fluorinated polymer, and a parylene.
4. The method of claim 3, wherein the step of forming the polymeric material comprises forming a polymeric material selected from the group of Type I polyimide, Type III polyimide, and Type V polyimide.
5. The method of claim 4, wherein the step of forming the polymeric material comprises forming a Type I polyimide.
6. The method of claim 4, wherein the step of forming the polymeric material comprises forming a fluorinated polyimide.

7. The method of claim 6, wherein the step of forming the polymeric material comprises forming a fluorinated Type I polyimide.

8. The method of claim 1, wherein the supercritical fluid is carbon dioxide.

9. The method of claim 8, wherein the step of converting the polymeric material comprises converting at least a portion of the polymeric material to a foamed polymeric material having a maximum cell size of less than about 1.0 micron.

10. The method of claim 9, wherein the step of converting the polymeric material comprises converting the polymeric material to a foamed polymeric material having a maximum cell size of less than about 0.1 micron.

11. The method of claim 1, wherein the converting step includes saturating the polymeric material with the supercritical fluid at or above the critical pressure and critical temperature for the supercritical fluid in a process chamber, and thereafter depressurizing the process chamber.

12. The method of claim 1, wherein the step of converting the polymeric material comprises converting at least a portion of the polymeric material to a foamed polymeric material having a maximum cell size of less than about 3.0 microns.

13. The method of claim 1, the method further comprising the step of forming a conductive layer adjacent the foamed polymeric material.

14. The method of claim 13, wherein the step of forming a conductive layer adjacent the foamed polymeric material comprises forming a metal line on the foamed polymeric material.

15. The method of claim 13, wherein the step of forming a conductive layer adjacent the foamed polymeric material comprises forming an interconnect selected from the group of a contact and a via adjacent the foamed polymeric material.

16. The method of claim 1, the method further comprising the steps of:

 patterning the foamed polymeric material resulting in exposed portions of the foamed polymeric material; and

 etching the exposed foamed polymeric material to form a patterned foamed polymeric layer.

17. The method of claim 16, wherein the etching step comprises using an oxygen plasma to etch the exposed foamed polymeric material.

18. A method of fabricating an interconnect for an integrated circuit, the method comprising the steps of:

 providing a substrate that includes an active area of the integrated circuit;

 forming a polymeric material on the substrate;

 converting at least a portion of the polymeric material formed on the substrate to a foamed polymeric material, wherein the step of converting the polymeric material comprises exposing at least a portion of the polymeric material to a supercritical fluid;

 defining at least one contact hole in the foamed polymeric material to the active area of the integrated circuit; and

 filling the contact hole with a conductive material.

19. The method of claim 18, wherein the step of forming a polymeric material on the substrate comprises forming a polyimide on the substrate.

20. The method of claim 18, the method further comprising the step of defining at least one trench in the foamed polymeric material, wherein at least a portion of the at least one trench is adjacent to at least a portion of the at least one

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contact hole, and further wherein the filling step includes filling the at least one contact hole and the at least one trench with the conductive material.

21. A method of fabricating an interconnect for an integrated circuit, the method comprising the steps of:

- providing a substrate that includes a conductive layer;
- forming a polymeric material on the conductive layer;
- converting at least a portion of the polymeric material formed on the conductive layer to a foamed polymeric material, wherein the step of converting the polymeric material comprises exposing at least a portion of the polymeric material to a supercritical fluid;
- defining at least one via in the foamed polymeric material; and
- filling the via with a conductive material.

22. The method of claim 21, wherein the step of forming a polymeric material on the substrate comprises forming a polyimide on the substrate.

23. The method of claim 21, the method further comprising the step of defining at least one trench in the foamed polymeric material, wherein at least a portion of the at least one trench is adjacent to at least a portion of the at least one via, and further wherein the filling step includes filling the at least one via and the at least one trench with the conductive material.

24. A method of forming an insulating material for use in an integrated circuit, the method comprising the steps of:

- providing a substrate of the integrated circuit;
- forming a layer of Type I polyimide on the substrate; and
- converting at least a portion of the Type I polyimide formed on the substrate to a foamed Type I polyimide, wherein the step of converting to a foamed Type I polyimide comprises exposing the Type I polyimide to a supercritical fluid.

25. The method of claim 24, wherein the step of forming the Type I polyimide comprises forming a Type I polyimide

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having a thickness of about 0.1 microns to about 1.0 microns and wherein the step of converting the Type I polyimide comprises converting to a foamed Type I polyimide having a thickness of about 0.2 microns to about 10 microns.

26. The method of claim 24, wherein the step of converting to a foamed polymeric material comprises exposing the Type I polyimide to supercritical carbon dioxide.

27. The method of claim 24, wherein the method further comprises the steps of patterning the foamed Type I polyimide and etching at least one of a contact hole, a via, or a trench in the foamed Type I polyimide.

28. The method of claim 27, the method further comprising the step of depositing a metal in the at least one of the contact hole, the via, or the trench.

29. The method of claim 24, wherein the step of converting to a foamed polymeric material comprises converting to a foamed polymeric material having a cell size of less than about 0.1 micron.

30. A method of forming an insulating material for use in an integrated circuit, the method comprising the steps of:

- providing a substrate of the integrated circuit;
- forming a layer of fluorinated polymer on the substrate; and

converting at least a portion of the fluorinated polymer formed on the substrate to a foamed fluorinated polymer, wherein the step of converting to a foamed fluorinated polymer comprises exposing the fluorinated polymer to a supercritical fluid.

31. The method of claim 30, wherein the step of forming a layer of fluorinated polymer includes forming a layer of a fluorinated polyimide.

32. The method of claim 31, wherein the step of forming a layer of fluorinated polyimide includes forming a layer of a fluorinated Type I polyimide.

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