

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KAMERAN AZADET, ISAAC M. LIVNY,
and ANIL MUDICHINTALA

Appeal 2008-2745
Application 10/924,280
Technology Center 2100

Decided: December 29, 2008

Before JOSEPH L. DIXON, HOWARD B. BLANKENSHIP, and
JAY P. LUCAS, *Administrative Patent Judges*.

BLANKENSHIP, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1, 2, 4-13, 15-20, and 22-24. Claims 3, 14, and 21 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Invention

Appellants' invention is directed to a peripheral controller (Fig. 3, 300; Spec. 3:26 - 4:4) comprising a controller (Fig. 2, 200) for controlling one or more peripheral devices; and a single interface (Fig. 5, 520) to a single shared memory device (Figs. 3 and 5, 320) that stores both configuration information (Fig. 4, 450) for the one or more peripheral devices and additional code (Fig. 4, 460), wherein the additional code is boot ROM code. (Spec 4:5-20).

Representative Claim

1. A peripheral controller, comprising:
a controller for controlling one or more peripheral devices; and
a single interface to a single shared memory device that stores both configuration information for said one or more peripheral devices and additional code, wherein said additional code is boot ROM code.

Prior Art

The Examiner relies on the following references as evidence of unpatentability:

Newman	2005/0198405 A1	Sep. 8, 2005
Getson	5,101,490	Mar. 31, 1992
Lindsay	2003/0014517 A1	Jan. 16, 2003
Wong	5,638,320	Jun. 10, 1997
Hameed	6,792,511 B2	Sep. 14, 2004
Rostoker	5,761,516	Jun. 2, 1998

Examiner's Rejections

Claims 1, 4, and 7 stand rejected under 35 U.S.C. § 103(a) based on the combination of Newman and Getson.

Claims 2 and 9 stand rejected under 35 U.S.C. § 103(a) based on the combination of Newman, Getson, and Lindsay.

Claim 5 stands rejected under 35 U.S.C. § 103(a) based on the combination of Newman, Getson, and Wong.

Claims 6 and 8 stand rejected under 35 U.S.C. § 103(a) based on the combination of Newman, Getson, and Hameed.

Claims 10-12, 15, 18, 20, and 23 stand rejected under 35 U.S.C. § 103(a) based on the combination of Newman, Getson, and Rostoker.

Claim 13 stands rejected under 35 U.S.C. § 103(a) based on the combination of Newman, Getson, Rostoker, and Lindsay.

Claim 16 stands rejected under 35 U.S.C. § 103(a) based on the combination of Newman, Getson, Rostoker, and Wong.

Claims 17, 19, 22, and 24 stand rejected under 35 U.S.C. § 103(a) based on the combination of Newman, Getson, Rostoker, and Hameed.

Claim Groupings

Based on Appellants' arguments in the Appeal Brief, we will decide the appeal on the basis of independent claim 1. Appellants group independent claims 1, 12, and 20 together (App. Br. 4-6), and rely on the arguments presented in support of claim 1 as response to the numerous rejections applied against other claims, thus waiving separate consideration of those claims. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUE

Have Appellants shown that the Examiner erred by finding that the combination of Newman and Getson teaches a single shared memory device that stores both boot ROM code and configuration information for one or more peripheral devices?

FINDINGS OF FACT

Appellants' Invention

1. The invention has a single shared memory device (Spec. 4:16-28; Fig. 3, 320).
2. In one configuration of the invention, two distinct memories may be employed as the single shared memory device (Spec. 4:29-30).
3. The claim term "memory" should be construed broadly enough to encompass any information able to be read from or written to an address in addressable space accessed by an associated processor (Spec. 5:13-15).

4. Information on a network is still within a memory because the associated processor can retrieve the information from the network (Spec. 5:15-16).

Newman

5. Newman discloses a controller for controlling one or more peripheral devices (Fig. 1, 100; Abstract).

6. The controller has a single interface to a single EEPROM memory device (Fig. 1, 106, 103; ¶ [0027]).

Getson

7. Getson discloses a controller for controlling one or more peripheral devices (Fig. 1, 1; Abstract).

8. Getson discloses a memory which stores both configuration information for peripheral devices and additional microinstruction code (Fig. 1, 20; Fig. 2; Abstract).

9. Getson discloses a memory which stores boot ROM code (Fig. 1, 22; Abstract).

10. The memories 20 and 22 encompass configuration information and boot ROM code information that is able to be read from or written to an address in addressable space by an associated processor (Abstract; col., 3 ll. 5-12).

PRINCIPLES OF LAW

Claim Interpretation

During examination, claims are to be given their broadest reasonable interpretation consistent with the specification, and the language should be read in light of the specification as it would be interpreted by one of ordinary

skill in the art. *In re American Academy of Science Tech Center*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (citations omitted). The Office must apply the broadest reasonable meaning to the claim language, taking into account any definitions presented in the specification. *Id.* (citing *In re Bass*, 314 F.3d 575, 577 (Fed. Cir. 2002)).

Obviousness

The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966).

The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1739 (2007).

ANALYSIS

Appellants contend that claim 1 distinguishes over the prior art because neither Newman nor Getson discloses or suggests a single shared memory device that stores both configuration information and boot ROM code as recited in claim 1. Specifically, Appellants contend that Getson discloses two different memory elements 20 and 22 that store configuration information and boot ROM code. Appellants further contend that the Examiner has not addressed how the two different memory elements 20 and 22 can be a single shared memory device (App. Br. 4-6).

Claim 1 does not require the single shared memory device to be a monolithic integrated circuit memory chip. In fact, one embodiment of Appellants' invention uses two distinct memories that share the same bus line as the single shared memory device. In another embodiment of Appellants' invention, a memory device encompasses any "information able to be read from or written to an address in the addressable space accessed by an associated processor." (FF 1-4).

A broad but reasonable interpretation of the term "single shared memory device" recited in claim 1 is a device storing "information able to be read from or written to an address in addressable space accessed by an associated processor." The memories 20 and 22 of Getson contain configuration and boot ROM code information that are "able to be read from or written to an address in addressable space accessed by an associated processor" (FF 8-10). Therefore, Getson discloses a single shared memory device that stores both configuration information for said one or more peripheral devices and additional code, wherein said additional code is boot ROM code.

Even if we assume that the "single shared memory device" of claim 1 distinguishes over memories 20 and 22 of Getson, the Examiner finds that a person of ordinary skill in the art at the time of invention would have found it obvious to store the configuration information and boot code taught by Getson in a single memory element as described by Newman, in order to provide a lower cost device (Ans. 15).

Appellants contend that a person of ordinary skill in the art would not ignore conventional wisdom and would not store the configuration information and boot code in the same memory element (Reply Br. 4-5).

Appellants have not, however, submitted any evidence in support of this alleged “conventional wisdom.” As support for the allegation, Appellants refer to the “Background of the Invention” in the Specification (at 1), which merely indicates what Appellants thought to be “typical” or “common.”

Appellants fail to address the Examiner’s finding that storing configuration information and boot code in a single memory element as described by Newman would provide a lower cost device. Moreover, the “Background” statement in Appellants’ Specification appears to be consistent with the Examiner’s finding. The asserted “typical” or “common” configuration is “contrary to the growing trends toward surface area and pin counts. A need therefore exists for a controller architecture that provides for a reduced surface area and pin count.” (Spec. 1:28-30).

Storing the configuration information and boot code disclosed by Getson in a memory element as disclosed by Newman appears to represent no more than the combination of familiar elements according to known methods, and Appellants have provided no evidence to the contrary. We are not persuaded that storing configuration information and boot code in the same memory element was “uniquely challenging or difficult for one of ordinary skill in the art,” (*see Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007) (citing *KSR*, 127 S. Ct. at 1741)), even assuming that claim 1 requires some kind of “memory element” such as a monolithic chip.

Therefore, Appellants haven not shown error in the Examiner’s initial showing of obviousness, and we sustain the rejection of independent claim 1, and of claims 2, 4-13, 15-20, and 22-24, which fall with claim 1.

CONCLUSIONS OF LAW

Appellants have not shown that the Examiner erred by finding that the combination of Newman and Getson teaches a single shared memory device that stores both boot ROM code and configuration information for one or more peripheral devices.

DECISION

We affirm the Examiner's rejection of claims 1, 2, 4-13, 15-20, and 22-24.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

msc

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