

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* KAISER H. WONG

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Appeal 2008-2997  
Application 10/284,557  
Technology Center 1700

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Decided: September 30, 2008

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Before CHUNG K. PAK, ROMULO H. DELMENDO, and  
JEFFREY T. SMITH, *Administrative Patent Judges*.

PAK, *Administrative Patent Judge*.

**DECISION ON APPEAL**

This is a decision on an appeal under 35 U.S.C. § 134 from the Examiner's final rejection of claims 1 through 20, all of the claims pending in the above-identified application. We have jurisdiction pursuant to 35 U.S.C. § 6.

We AFFIRM.

*STATEMENT OF THE CASE*

The subject matter on appeal relates to a method of copper electroplating a transistor structure. (Spec. 2, 5). In one embodiment illustrated in Figures 3 and 4, a dielectric layer (e.g., a layer containing an oxide layer 32, a nitride layer 34, and a field oxide layer 36) is formed on the top surface of a silicon wafer 46. (Spec. 4, 5 and originally filed claim 20). After forming a trench 10 and a via 50 in the dielectric layer, a diffusion barrier layer composed of tantalum is selectively deposited on the surfaces of the via 50 and trench 10. (Spec. 5).

The transistor structure is then immersed in a plating bath containing a cupric ion solution 52 for electroplating, where a negative terminal of a power supply connects to a metal layer located at the bottom of the wafer. *Id.* When powered on, cupric ions are reduced to form copper atoms, and deposited on the barrier layer inside the trench 10. (Spec. 4, 5). The power to the plating bath is terminated when the copper atoms fill the trench 10. (Spec. 5). Although Appellant's Figures 3 and 4 illustrate a single copper layer formed directly on the barrier layer and having a height extending to the top of the trench as the preferred single copper layer formed directly on the barrier layer, the Specification as a whole does not limit the claimed "copper electroplating a single layer directly on the barrier layer" recited in claims 1, 12, and 20 to such single copper layer. *See, e.g., Spec. 5.*

Further details of the appealed subject matter are recited in representative claims 1, 12, and 20, which are reproduced below:

1. A copper electroplating method for fabrication of copper interconnect for integrated circuits including a dielectric layer, comprising:
  - providing a silicon wafer having a bottom metal layer;
  - forming the dielectric layer on the silicon wafer;
  - forming a trench and via on the silicon wafer;
  - forming a barrier layer on the wafer as a pattern that defines the trench and via but does not cover a top surface of the dielectric layer;
  - connecting a negative terminal of a power supply to contact the bottom metal layer of the wafer, the bottom metal layer located on a side of the wafer opposite to the trench and via; and
  - copper electroplating in a single layer directly on the barrier layer to the top of the trench;
  - terminating a power to the copper electroplating when the copper electroplating and barrier layer have planar top surfaces occupying a single plane that also includes the top surface of the dielectric layer.
  
12. A copper electroplating method for fabrication of copper interconnect for integrated circuits including a dielectric layer, comprising:
  - providing a transistor structure that includes a bottom metal layer;
  - forming a source, a drain, a gate electrode and the dielectric layer on the transistor structure;
  - forming a trench and via on the transistor structure;
  - forming a barrier layer as a pattern that defines the trench and via but does not cover a top surface of the dielectric layer on the transistor structure;
  - connecting a negative terminal of a power supply to contact the bottom metal layer of the transitor [sic., transistor] structure, the bottom metal layer located on a side of the transistor structure opposite to the trench and via; and
  - copper electroplating in a single layer directly on the barrier layer formed to the top of the trench;
  - terminating a power to the copper electroplating when the copper electroplating and barrier layer have planar top surfaces occupying a single plane that also includes the top surface of the dielectric layer.

20. A copper electroplating method for fabrication of copper interconnect for integrated circuits including a dielectric layer, comprising:

providing a substrate having a bottom metal layer;

forming a source, a drain, a gate electrode and the dielectric layer on the substrate;

forming a trench and via above the substrate;

forming a barrier layer above the substrate as a pattern that defines the trench and via but does not cover a top surface of the dielectric layer;

connecting a negative terminal of a power supply to contact the bottom metal layer of the substrate, the bottom metal layer located on a side of the substrate opposite to the trench and via; and

copper electroplating in a single layer directly on the barrier layer to the top of the trench;

terminating a power to the copper electroplating when the copper electroplating and barrier layer have planar top surfaces occupying a single plane that also includes the top surface of the dielectric layer; wherein tantalum is used as the barrier layer along with field oxide, nitride and oxide layers as the dielectric layer to form the trench and via above the substrate.

As evidence of unpatentability of the claimed subject matter, the Examiner relies upon the following references:

Mackintosh	3,391,035	Jul. 2, 1968
Asami	4,065,374	Dec. 27, 1977
Fujihira	5,053,838	Oct. 1, 1991
Zhang	5,893,752	Apr. 13, 1999
Yu	6,287,968 B1	Sep. 11, 2001
Wang '295	6,440,295 B1	Aug. 27, 2002

As evidence of patentability of the claimed subject matter, Appellant relies upon the following reference:

Wang '166	6,391,166 B1	May 21, 2002
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The Examiner rejects the claims on appeal as follows:

- 1) Claims 1-11 under 35 U.S.C. § 103(a) as unpatentable over the combined disclosures of Yu, Mackintosh, Asami, Wang '295, Zhang, and Fujihira;
- 2) Claims 12-19 under 35 U.S.C. § 103(a) as being unpatentable over the combined disclosures of Yu, Mackintosh, Asami, Wang '295, Zhang, and Fujihira; and
- 3) Claim 20 under 35 U.S.C. § 103(a) as being unpatentable over the combined disclosures of Yu, Mackintosh, Asami, Wang '295, Zhang, and Fujihira.

#### ISSUE

Appellant does not dispute the Examiner's determination that Yu, in combination with the other applied references, would have suggested sequentially forming a dielectric layer, a trench, a via, a barrier layer, and a copper seed layer on a silicon wafer and connecting a negative terminal of a power supply to a metal layer located at the bottom of the wafer as required by claim 1. (*Compare Ans. 3-27 with App. Br. 11-17 and Reply Br. 1-6; see FF 1-7 below*).

Appellant only argues (App. Br. 11 and 13-14) that "none of the enumerated references teaches or suggests . . . a metal [copper] layer can be formed directly on a barrier layer in a single layer" and that Yu alone, or in combination with the other applied references, does not teach, nor would have suggested, the limitation "terminating a power of the copper electroplating when the copper electroplating and barrier layer have planar

top surfaces occupying a single plane that also includes the top surface of the dielectric layer" recited in claim 1.

The dispositive issue is, therefore, has Appellant shown reversible error in the Examiner's determination that Yu, in combination with the other applied references, such as Wang '295, would have suggested the limitations "copper electroplating in a single layer directly on the barrier layer to the top of the trench" and "terminating a power of the copper electroplating when the copper electroplating and barrier layer have planar top surfaces occupying a single plane that also includes the top surface of the dielectric layer" recited in claim 1 within the meaning of 35 U.S.C. § 103.

#### RELEVANT FINDINGS OF FACT (FF)

##### 1. Claim 1 of Yu recites that:

A method of manufacturing a semiconductor wafer, the method comprising:  
forming a partially completed semiconductor wafer having at least one trench formed in a layer of interlayer dielectric;  
forming a conformal barrier layer on a surface of the interlayer dielectric including walls of the at least one trench;  
forming a conformal seed layer on the barrier layer;  
forming a layer of photoresist on the conformal seed layer;  
patterning and developing the layer of photoresist exposing portions of the conformal seed layer;  
etching away the exposed portions of the conformal seed layer and the underlying conformal barrier layer thereby negating a requirement for a chemical mechanical polishing process;  
removing the layer of photoresist from the at least one trench; and  
filling the at least one trench with the conductive material by a method selected from the group of electroplating and electroless plating, wherein a top surface of the conductive material is

substantially planar with the surface of the interlayer dielectric thereby negating a requirement for a chemical mechanical polishing process to remove excess conductive material.

2. Claim 2 of Yu recites, "[t]he method of claim 1 wherein the step of filling the at least one trench with the conductive material is accomplished by filling the at least one trench with copper."
3. Yu teaches (col. 1, ll. 55-57) the barrier layer is typically formed from a metallic nitride material such as TiN or TaN.
4. Yu teaches (col. 5, l. 58 to col. 6, l. 11) a copper seed layer 328 is formed on a barrier layer 326 via an electroplating process.
5. Mackintosh at col. 1, ll. 25-30 states, "[i]n any integrated circuit, it is necessary to start with a wafer of semiconductor material of one conductivity type. For example, the starting material may be a wafer of P-type silicon."
6. Asami teaches (col. 1, ll. 39-45 and col. 5, ll. 50-55) an electroplating method for the preparation of "Planar or Mesa type semiconductors having diffusion zones with metal on every diffusion zone, in a plating process to prepare said semiconductor zone for providing electrodes."
7. Asami at col. 8, ll. 46-60 states:

In FIG. 3 the wafer **3** is illustrated on an enlarged scale. The wafer **3** comprises a base plate 31, for example, of N<sup>+</sup> silicon supporting a layer **32** of N- silicon. The layer **32** is formed by epitaxial growth. An insulating covering layer **33** of silicon dioxide is formed on the layer **32** and provided with windows **34**. The windows may be formed by photoetching techniques well known in the art. P-type zones **35** are formed by diffusion of a P-type impurity into the N- silicon layer **32** through the windows **34**. A metallic layer **36** of positive polarity is prepared on every p-type

zone **35** in order to assure a sufficiently strong bonding between the zone **35** and the respective "bump" to be provided in the window areas by the plating. On the back of the N+ silicon base plate 31, a layer of gold **37** and a layer of silver **38** are applied by a plating process to form a metallic cathode layer.

8. Asami at col. 4, ll. 45-60 states:

According to the invention, the plating current density is maintained constant regardless of the increase of the surface area being plated as the "bump" plating of a hemispherical configuration progresses. This is accomplished, according to the invention, by controlling the plating current by a computer program which takes into account the relationship between the surface area and a plating type previously determined by experimentation. Simultaneously, the plating current to the standard electrode is also controlled or regulated and a constant current source is employed in order to adjust or compensate for any change of current density due to surface area changes which cannot be anticipated by preliminary experiments. The change of the conductivity of the electrolytic solution is also taken into account as a control or regulating factor.

9. Asami at col. 10, ll. 4-6 states, "no plating metal deposits could be found in any locations where such deposits are not desired."
10. Wang '295 at col. 8, ll. 8-15 states, "[m]etal layer **121** can be formed on barrier layer **122** or on dielectric layer **123** using . . . an electroplating [process] . . ."
11. Wang '295 at col. 8, ll. 2-7 teaches that the metal layer 121 may include, *inter alia*, copper.
12. Wang '295 at Fig. 1A and col. 7, ll. 29-65 teaches, *inter alia*, filling trenches 125, which are coated with a barrier layer 122, with a single copper layer 121 via copper electroplating.

13. This method of filling trenches with a single copper layer 121 does not require additional steps, such as copper electroplating a copper seed layer. *See* Wang Fig. 1A and col. 7, ll. 29-65.
14. Wang '295 teaches at col. 7, ll. 45-50 that barrier layer 122 may be composed of TiN.
15. Wang '166 at col. 19, ll. 7-19 states:

Process Steps for Plating Conductive Film (or Seed Layer)  
Directly on Barrier Layer.

Step 1: Turn on LMFC **21** only, so that electrolyte only touches a portion of wafer **31** above anode **3**. Step 2: After the flow of electrolyte is stabilized, turn on power supply **11**. Positive metal ion will be plated onto portion area of wafer **31** above anode **3**.

Step 3: When the thickness of the metal conductive film reaches the set-value or thickness, turn off power supply **11** and turn off LMFC **21**.

Step 4: Repeat step 1 to 3 for anode **2**, using LMFC **22** and power supply **12**.

Step 5: Repeat step 4 for anode **1**, using LMFC **23** and power supply **13**.

## PRINCIPLES OF LAW

When a claim employs the transitional term "comprising," it is interpreted as not precluding the presence of additional ingredients and/or steps which are not recited. *In re Baxter*, 656 F.2d 679, 686-87 (CCPA 1981).

Under 35 U.S.C. § 103, the factual inquiry into obviousness requires a determination of: (1) the scope and content of the prior art; (2) the differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) secondary considerations, if any. *Graham*

v. *John Deere Co.*, 383 U.S. 1, 17-18 (1966). “[A]nalysis [of whether the subject matter of a claim would have been obvious] need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007).

These inferences and creative steps may include economic factors. See *In re Thompson*, 549 F.2d 1290, 1294 (CCPA 1976), *In re Clinton*, 527 F.2d 1226, 1229 (CCPA 1976).

## ANALYSES

### *Rejection (1): Claims 1-11 under §103<sup>1</sup>*

Yu teaches copper electroplating a copper seed layer directly on a TiN barrier layer of a partially completed semiconductor wafer 300. (FF 1, 3-4). Yu also teaches copper electroplating an additional layer of copper on top of the copper seed layer via electroplating "wherein a top surface of the conductive material [i.e., copper] is substantially planar with the surface of the interlayer dielectric thereby negating a requirement for a chemical mechanical polishing process to remove excess conductive material." (FF 1-4). Indeed, Asami also teaches using a computer to control the plating current, which is known to be a function of power, in an electroplating

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<sup>1</sup> Appellant does not separately argue the individual claims on appeal. Therefore, we select claim 1 as the representative claim consistent with 37 C.F.R. § 41.37(c)(1)(vii).

process so that "no plating metal deposits. . . [are] found in any locations where such deposits are not desired." (FF 8-11).

Wang '295, like Yu and Asami, teaches electroplating a conductive material to form a semiconductor component. (FF 1-4 and 6-11). Wang '295 also teaches copper electroplating a single copper layer 121 to fill trenches, which have a TiN barrier layer. (FF 10-13). This method of filling the trenches, as is readily appreciated by one of ordinary skill in the art via simple observation, is advantageous in that it does not require additional steps, such as the electroplating a copper seed layer taught by Yu. (FF 14).

Given the above teachings, we concur with the Examiner that Yu, in combination with the other applied references, such as Wang '295 and Asami, would have suggested copper electroplating in a single layer directly on the barrier layer to the top of the trench and terminating a power of the copper electroplating when the copper electroplating and barrier layer have planar top surfaces occupying a single plane, motivated by a reasonable expectation of successfully eliminating the need for copper electroplating a seed layer and chemical mechanical polishing of excess copper materials.

As a rebuttal to the *prima facie* case of obviousness established by the Examiner, Appellant alleges that Wang '166, which is incorporated by reference in Wang '295, shows that Wang '295 does not teach that a single metal (copper) layer can be formed directly on a barrier layer to the top of the trench. (Br. 11) In this regard, Appellant alleges that Wang '166 teaches turning power on and off to adjust the thickness of layers succeeding a single seed layer. (Br. 12). Thus, according to Appellant, it is unreasonable to assert that Wang '295 teaches copper electroplating in a single layer directly

on the barrier layer to the top of the trench because Wang '295, as explained by Wang '166, explicitly discloses electroplating multiple copper layers to fill trenches. (Br. 12). We do not agree.

Contrary to Appellant's assertions, we find that Wang '166, in explaining Wang '295, teaches electroplating a single layer and not multiple layers stacked on top of each other. Wang '166 teaches a process for plating a single conductive film directly on a barrier layer by forming a conductive film on a portion of the wafer 31 via a liquid flow mass controller (LMFC) 21. (FF 12). Wang '166 teaches that when the conductive film reaches its desired height, the power to LMFC 21 is turned off and the power to LMFC 22 is turned on in order to plate another portion of the wafer 31. *Id.* Thus, what Wang '166 teaches is that the LMFC plates a single conductive film on a section of the wafer as each LMFC operates on a different section of the wafer. Therefore, we are not convinced that Wang '295, as explained by Wang '166, does not teach the claimed single copper layer electroplating. From our perspective, Wang '166 simply does not negate the teachings of Wang '295 as discussed above.

Accordingly, based on the Factual Findings set forth above and in the Answer, we concur with the Examiner that Yu, Mackintosh, Asami, and Wang '295 render the subject matter defined by claims 1-11 obvious within the meaning of 35 U.S.C. § 103(a)<sup>2</sup>.

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<sup>2</sup> We note that a discussion of Zhang and Fujihira is unnecessary to resolve the issue raised.

*Rejection (2): Claims 12-19 under §103<sup>3</sup>*

The Examiner determines that Yu, Mackintosh, Asami, Wang '295, Zhang, and Fujihira would have rendered the subject matter covered by claim 12 obvious to one of ordinary skill in the art. (Ans. 15-16). Appellant repeats the same arguments directed to rejection (1) above<sup>4</sup> (Br. 15). Thus, based on the same Factual Findings and conclusions set forth above and in the Answer, we concur with the Examiner that Yu, Mackintosh, Asami, Wang '295, Zhang, and Fujihira would have rendered the subject matter recited in claims 12-19 obvious to one of ordinary skill in the art within the meaning of 35 U.S.C. § 103(a).

Accordingly, we affirm the Examiner's decision rejecting claims 12-19 under 35 U.S.C. § 103(a).

*Rejection (3): Claim 20 under §103*

The Examiner finds that Yu, Mackintosh, Asami, Wang '295, Zhang, and Fujihira would have rendered the subject matter covered by claim 20 obvious to one of ordinary skill in the art. (Ans. 26-27). Appellant repeats

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<sup>3</sup> Appellant does not separately argue the individual claims on appeal. Therefore, we select claim 12 as the representative claim consistent with 37 C.F.R. § 41.37(c)(1)(vii).

<sup>4</sup> The limitations "copper electroplating in a single layer directly on the barrier layer to the top of the trench" and "terminating a power of the copper electroplating when the copper electroplating and barrier layer have planar top surfaces occupying a single plane that also includes the top surface of the dielectric layer" recited in independent claim 1 are also recited in independent claim 12.

the same arguments directed to rejection (1) above,<sup>5</sup> (App. Br. 16). Thus, based on the same Factual Findings and conclusions set forth above and in the Answer, we concur with the Examiner that Yu, Mackintosh, Asami, Wang '295, Zhang, and Fujihira would have rendered the subject matter recited in claims 12-19 obvious to one of ordinary skill in the art within the meaning of 35 U.S.C. § 103(a).

Accordingly, we affirm the Examiner's decision rejecting claims 12-19 under 35 U.S.C. § 103(a).

*ORDER*

The decision of the Examiner is affirmed.

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<sup>5</sup> The limitations "copper electroplating in a single layer directly on the barrier layer to the top of the trench" and "terminating a power of the copper electroplating when the copper electroplating and barrier layer have planar top surfaces occupying a single plane that also includes the top surface of the dielectric layer" recited in independent claim 1 are also recited in independent claim 12.

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*TIME PERIOD*

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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