

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte VICTOR PROKOFIEV

Appeal 2008-3248
Application 10/787,681
Technology Center 2800

Decided: October 20, 2008

Before ROBERT E. NAPPI, JOHN A. JEFFERY, and MARC S. HOFF,
Administrative Patent Judges.

JEFFERY, *Administrative Patent Judge.*

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134 from the Examiner's rejection of claims 1-4, 11, 12, 20-24, and 29. We have jurisdiction under 35 U.S.C. § 6(b). We REVERSE.

STATEMENT OF THE CASE

Appellant invented a method, socket, and socket integrated circuit package. The method, socket, and package include a socket pin with spring arms extending away from one another and fitting into a via located in an integrated circuit package. The opposed end of the pin may also have a pair of spring arms to connect the integrated circuits to the printed circuit boards.¹ Independent claim 1 is reproduced below:

1. A method comprising:

inserting a socket pin including at least two resilient spring arms extending away from one another into a via in an integrated circuit package.

The Examiner relies upon the following as evidence in support of the rejection:

Mogi	US 4,872,850	Oct. 10, 1989
------	--------------	---------------

(1) Claims 1-4, 20-24, and 29 stand rejected under 35 U.S.C. § 102(b)² as being anticipated by Mogi.

(2) Claims 11 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mogi.

¹ See generally Spec. 2:13-3:16 and 4:23-27.

² The Examiner acknowledges on page 4 of the Answer the typographical error in the Office Action that based the rejection on paragraph (e) of section 102. The grounds of the rejection is actually based on 35 U.S.C. § 102(b). Additionally, we presume the Examiner intended to refer to the Final Office Action mailed November 6, 2006 and not the Advisory Action mailed April 4, 2007, which contains no rejection or reference to paragraph (e) of section 102.

Rather than repeat the arguments of Appellant or the Examiner, we refer to the Briefs³ and the Answer⁴ for their respective details. In this decision, we have considered only those arguments actually made by Appellant. Arguments, which Appellant could have made but did not make in the Briefs, have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Claims 1-4, 20-24, and 29

We first turn the rejection of independent claim 1 under 35 U.S.C. § 102(b) as being anticipated by Mogi. The Examiner finds that Mogi discloses all the recited elements (Ans. 4). Appellant argues that the anticipation rejection improperly relies on common knowledge (App. Br. 10; Reply Br. 1-2) and that Mogi does not disclose the spring arms extending into a via in an integrated circuit package (App. Br. 10; Reply Br. 2).

ISSUE

The following issue has been raised in the present appeal:

Whether Appellant has shown that the Examiner erred in finding that Mogi discloses two resilient spring arms extending into a via in an integrated circuit package.

³ We refer to the Appeal Brief filed June 21, 2007, and the Reply Brief filed October 9, 2007, throughout this opinion.

⁴ We refer to the Examiner's Answer mailed August 31, 2007, throughout this opinion.

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. Mogi discloses an integrated circuit (IC) tester socket with a pin 6 having two resilient spring arms 6-1 and 6-2 (Mogi; col. 4, ll. 22, 35, 54-56 and col. 7, ll. 2-5; Figs. 5A-8).
2. Mogi discloses the IC tester socket includes an IC package P, a socket body 1, a spacing frame 2, and an urging cover 3 (Mogi, col. 3, ll. 51-55 and col. 4, ll. 24-29; Figs. 3-4).
3. Mogi discloses the socket body 1, the spacing frame 2, and the urging cover 3 are made from PPS resin (Mogi, col. 4, ll. 48-52).
4. Mogi discloses the arms 6-1 and 6-2 of the pin extend into a groove or recess of spacing frame 2 and urging cover 3 (Mogi, col. 5, ll. 26-68; Figs. 5A-C).
5. The Specification does not define the term, “via.”
6. A via is defined as a “[v]ertical opening filled with conducting material used to connect circuits on various layers of a device to one another and to the semiconductor substrate.”⁵

⁵ Peter Van Zant, MICROCHIP FABRICATION 629 (5th ed. 2004). See Evidence Appendix, *supra*, of this decision.

7. The Wiley Encyclopedia of Electrical and Electronics Engineering also shows and describes through hole vias, blind vias, and microvias in different layers of electronic packaging.⁶
8. A polyphenylene sulfide (PPS) resin is an insulating material. *See, e.g.,* U.S. Patent No. 6,552,273 B2 (col. 2, ll. 35-38), U.S. Patent No. 5,527,189 (col. 2, ll. 57-65), and U.S. 6,468,101 B2 (col. 5, ll. 45-48).
9. Mogi includes arms 6-1 and 6-2 on one end of pin 6 so that the IC package is properly mounted to come in contact with lead terminal R of the package during testing (Mogi, col. 5, ll. 26 - col. 6, ll. 2).
10. The Specification explains that the biased spring arms on opposed ends are meant “to engage the package 34 above and the board 42 below” (Spec. 4:23-24).

PRINCIPLES OF LAW

“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987).

⁶ Jad S. Rasul, *Printed Wiring Board Technology*, in WILEY ENCYCLOPEDIA OF ELECTRICAL AND ELECTRONICS ENGINEERING, Dec. 27, 1999, at 4-7, available at <http://mrw.interscience.wiley.com/emrw/9780471346081/eeee/article/W2110/current/pdf> (last visited Sept. 16, 2008). *See* Evidence Appendix, *supra*, of this decision.

During examination of a patent application, a claim is given its broadest reasonable construction “in light of the specification as it would be interpreted by one of ordinary skill in the art.” *In re Am. Acad. Of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004). “[T]he words of a claim ‘are generally given their ordinary and customary meaning.’” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted). “[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, *i.e.*, as of the effective filing date of the patent application.” *Id.* at 1313.

Discussing the question of obviousness of a patent that claims a combination of known elements, *KSR Int’l v. Teleflex, Inc.*, 127 S. Ct. 1727 (2007), explains:

When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida* [*v. AG Pro, Inc.*, 425 U.S. 273 (1976)] and *Anderson's-Black Rock[, Inc. v. Pavement Salvage Co.*, 396 U.S. 57 (1969)] are illustrative—a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

KSR, 127 S. Ct. at 1740.

ANALYSIS

Appellant first argues that the anticipation rejection improperly relies on common knowledge to meet the limitation of the spring arms at each of opposed end (App. Br. 10; Reply Br. 1-2). We do not agree. First, claim 1 recites “at least two resilient spring arms extending away from one another” and, therefore, the argument that the arms are at “opposed ends” is not commensurate in scope. This limitation, however, is in claim 11. Second, page 2 of the Final Office Action and pages 4 and 5 of the Answer clearly state claim 1 is rejected under 35 U.S.C. § 102. While we acknowledge that the Response to the Arguments section of the Final Office Action addresses common knowledge, this discussion does not form part of the anticipation rejection of claim 1.

Appellant also contends that Mogi does not disclose or teach “inserting a pin including two resilient arms extending away from one another into a via in an integrated circuit package”⁷ (App. Br. 10) or “there is no inserting of pins into vias in the package (Reply Br. 2). We agree for the below reasons.

The Examiner finds that the IC package P, the spacing frame 2, and the urging cover 3 of Mogi meet the limitation of the claimed IC package and that the inner sidewalls of the frame 2 and cover 3 form the vias (Ans. 4). The Specification has not defined a via (FF 5). However, terms are given their broadest reasonable construction in light of the specification and as the term would be interpreted by one of ordinary skill in the art. We thus

⁷ This argument was presented under the discussion of claims 11 and 12 (App. Br. 10). Since the quoted limitation is found in claim 1, we will presume that Appellant intended to include this argument for claim 1.

need to determine the ordinary and customary meaning the term “via” would have to a person of ordinary skill in the art at the time of the invention.

In the context of an IC package, a via has been defined as a “[v]ertical opening filled with conducting material used to connect circuits on various layers of a device to one another and to the semiconductor substrate” (FF 6). Vias are also shown and described as through hole vias, blind vias, and microvias in different layers of electronic packaging (FF 7). We, thus, find that the ordinary and customary meaning of the term, “via,” to a person of ordinary skill in the art is a conductive, vertical opening used to connect circuits on different layers of electronic packaging to one another.

Mogi discloses the spring arms 6-1 and 6-2 extend into grooves or recesses of the spacing frame 2 and the urging cover 3 (FF 1, 2, and 4). These recesses and grooves are not vertical openings. Additionally, the frame and cover are made from PPS resin (FF3), which is an insulating material (FF 8). The grooves and recesses of the frame 2 and cover 3 of Mogi are, therefore, not conductive, vertical openings or a vias on different layers of electronic packaging. Moreover, because the grooves and recesses are not vias, Mogi fails to disclose the spring arms 6-1 and 6-2 of Mogi extend into a via of electronic packaging as recited in claim 1.

As independent claim 20 recites “a plurality of vias on said integrated circuit package,” we also find that Mogi does not disclose the “plurality of vias on said integrated package” limitation of claim 20.

For the above reasons, Appellant has shown the Examiner erred in rejecting claim 1-4, 20-24, and 29 under 35 U.S.C. § 102(b) based on Mogi.

Claims 11 and 12

We next turn the rejection of claims 11 and 12 under 35 U.S.C. § 103(a) as being unpatentable over Mogi. Claim 11 recites a socket having a pin with a pair of spring biased spring arms on each of two opposed ends. The Examiner finds that Mogi combined with common knowledge teach all the recited elements (Ans. 4-5). Appellant argues that: (1) spring arms on opposed ends of a pin are not well known and (2) citation to Wang is not relevant (App. Br. 10-11).

The Examiner finds that including spring arms at opposed ends is well known and widely used in the electrical connector art to connect a device on opposed ends (Ans. 4-5). We do not agree. The Court in *KSR*, 127 S. Ct. at 1740-41, does state that “background knowledge possessed by a person having ordinary skill in the art” should be used in determining “whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” Additionally, “the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *KSR*, 127 S. Ct. at 1741. However, the notice of facts beyond the record which may be taken by the Examiner must be “capable of such instant and unquestionable demonstration as to defy dispute.” *In re Ahlert*, 424 F.2d 1088, 1091 (CCPA 1970) (citing *In re Knapp Monarch Co.*, 296 F.2d 230 (CCPA 1961)).

The Examiner has not provided any evidence or sufficient analysis for concluding that that one skilled in the art would have recognized the feature of spring arms on opposed ends of a socket pin is well known in the art. Although the Examiner cites Wang (U.S. Patent No. 6,186,797 B1) on page

3 of the Final Office Action to show that spring arms on opposed ends of a pin are well known, the Examiner's Answer clearly articulates that Wang forms no part of the obviousness rejection (Ans. 5). As this reference was not relied upon in the rejection⁸, Wang is not before us. Thus, the Examiner has not provided us with any evidence that is capable of such instant and unquestionable demonstration that having spring arms on opposed ends of a pin is well known.

Moreover, we fail to find a sufficient explanation for placing a pair of spring arms on each of two opposed ends of the socket pin in Mogi so as "to connect to a device on opposed ends" (Ans. 5). Mogi includes arms 6-1 and 6-2 on one end of the pin so that the IC chip package is properly mounted to come in contact with lead terminal R of the package during testing (FF 9). In contrast, the leg portion 6-3 in Mogi fits in a groove 12 of the socket body and extends outwardly as shown in Figure 4. There is no discussion or teaching that the opposed end or the leg portion 6-3 needs to be manipulated like arms 6-1 and 6-2. Additionally, there is no discussion or suggestion in Mogi that the leg portion 6-3 of pin 6 connects to another device. We, therefore, fail to see how one skilled in the art would have recognized a pair of biased spring arms on the opposed end or around leg portion 6-3 would improve or solve the problem of connecting the leg portion 6-3 to another device or yield a predictable variation of the proposed connection. *KSR*, 127 S. Ct. at 1739-40.

⁸ See *In re Hoch*, 428 F.2d 1341, 1342 n.3 (CCPA 1970) ("Where a reference is relied on to support a rejection, whether or not in a 'minor capacity,' there would appear to be no excuse for not positively including the reference in the statement of the rejection.").

Lastly, we are not persuaded that the duplication of arm 6-3 on the end of the connector pin 6 of Mogi would have involved only routine skill (Ans. 5). The court in *St. Regis Paper Co. v. Bemis Co., Inc.*, 549 F.2d 833, 838 (7th Cir. 1977) held that unless the combination of known elements in the prior art creates a synergistic result, the invention cannot be patented. In contrast to the present case, Mogi does not demonstrate that having biased spring arms on the opposed ends of a pin is known in the prior art. Thus, Mogi does not even teach a combination of known elements. Moreover, the Specification explains that the biased spring arms on opposed ends are meant “to engage the package 34 above and the board 42 below” (FF 10). As stated previously, Mogi does not teach or suggest that the leg portion 6-3 of pin 6 that extends below the socket body 1 is connected to any device such that there would have been a reason to duplicate the leg portion 6-3 or make the leg portion into a pair of spring biased arms as recited in claim 11.

For the above reasons, Appellant has shown the Examiner erred in rejecting claims 11 and 12 based on the teachings of Mogi.

CONCLUSION

(1) For the foregoing reasons, Appellant has shown the Examiner erred in finding that Mogi discloses a via in or on an integrated circuit.

(2) For the foregoing reasons, Appellant has shown the Examiner erred in finding Mogi combined with common knowledge teaches the feature of including a pair of biased spring arms on each of two opposed ends as recited in claim 11.

Appeal 2008-3248
Application 10/787,681

DECISION

We have not sustained the Examiner's rejection of claims 1-4, 11, 12, 20-24, and 29. Accordingly, the Examiner's rejections of claims 1-4, 11, 12, 20-24, and 29 are reversed.

REVERSED

eld

TROP PRUNER & HU, PC
1616 S. VOSS ROAD, SUITE 750
HOUSTON, TX 77057-2631

Appeal 2008-3248
Application 10/787,681

EVIDENCE APPENDIX

PETER VAN ZANT, MICROCHIP FABRICATION 629 (5th ed. 2004).

Jad S. Rasul, *Printed Wiring Board Technology*, WILEY ENCYCLOPEDIA OF ELECTRICAL ENGINEERING, December 27, 1999 at 4-7.

Microchip Fabrication

A Practical Guide to Semiconductor Processing

Peter Van Zant

Fifth Edition

McGraw-Hill

New York Chicago San Francisco Lisbon London Madrid
Mexico City Milan New Delhi San Juan Seoul
Singapore Sydney Toronto

Library of Congress Cataloging-in-Publication Data

Van Zant, Peter.

Microchip fabrication / Peter Van Zant.—5th ed.

p. cm.

Includes index.

ISBN 0-07-143241-8

1. Semiconductors—Design and construction. 2. Integrated circuits—Design and construction. I. Title.

TK7871.85.V36 2004
621.3815'2—dc22

2004040287

Copyright © 2004, 2000, 1997, 1984 by The McGraw-Hill Companies, Inc. All rights reserved. Printed in the United States of America. Except as permitted under the United States Copyright Act of 1976, no part of this publication may be reproduced or distributed in any form or by any means, or stored in a data base or retrieval system, without the prior written permission of the publisher.

1 2 3 4 5 6 7 8 9 0 DOC/DOC 0 1 0 9 8 7 6 5 4

ISBN 0-07-143241-8

The sponsoring editor for this book was Stephen S. Chapman and the production supervisor was Pamela Pelton. It was set in Century Schoolbook by J. K. Eckert & Company, Inc.

Printed and bound by R. R. Donnelley.

McGraw-Hill books are available at special quantity discounts to use as premiums and sales promotions, or for use in corporate training programs. For more information, please write to the Director of Special Sales, McGraw-Hill Professional, Two Penn Plaza, New York, NY 10121-2298. Or contact your local bookstore.

This book is printed on recycled, acid-free paper containing a minimum of 50% recycled, de-inked fiber.

Information contained in this work has been obtained by The McGraw-Hill Companies, Inc. ("McGraw-Hill") from sources believed to be reliable. However, neither McGraw-Hill nor its authors guarantee the accuracy or completeness of any information published herein and neither McGraw-Hill nor its authors shall be responsible for any errors, omissions, or damages arising out of use of this information. This work is published with the understanding that McGraw-Hill and its authors are supplying information but are not attempting to render engineering or other professional services. If such services are required, the assistance of an appropriate professional should be sought.

This edition is dedicated to two exceptional women, Marilyn (Van Zant) O'Connor and Anne Miller. Marilyn is my lovely and loving sister. She is also my good friend, enthusiastic supporter, and a wise confidant. Thanks, sis.

For over twenty years Anne has been a collaborator, business partner, and friend. Her wise business counsel and contributions to this text are greatly appreciated.

Preface to the Fifth Edition

Despite recessions, the microchip industry continues its evolutionary march to the physical limits of silicon-based ICs. Fortunately, the end seems always just over the hill, and the industry keeps chugging along. Unfortunately, keeping a textbook current with the advances in microchip fabrication means frequent updates. Hence this fifth edition.

This edition follows the same chapter sequence as the previous editions. Hopefully, this will assist instructors in upgrading their course curriculums. Fortunately, the basics of semiconductor device operation and wafer processing remain the same and will be found in this edition.

My thanks go to Steve Chapman, my editor at McGraw-Hill. His guidance and patience with my writing schedule are appreciated.

Many thanks to Anne Miller and Michael Heynes of Semiconductor Services for their consultation and input. Alex Braun, of Semiconductor International, and Nikki Wood, of Future Fab International, were most helpful with securing permission to reproduce material from their fine publications. Jeff Eckert, of J. K. Eckert & Co., did a fine job on organizing the over 600 figures and editing the manuscript. Mark Hall, Mark Hall Design, and David Wellner did yeoman's work transforming my hand drawings into understandable illustrations.

Last, but not least, thanks to my wife Mary Dewitt for enduring my 5:30 A.M. writing sessions and her unending support.

About the Author

Peter Van Zant is an internationally known semiconductor professional with an extensive background in process engineering, training, consulting, and writing. Principal of Peter Van Zant Associates, a firm that supplies writing, training, and consulting services to business and industry, he is the author of *Semiconductor Technology Glossary*, Third Edition; *Integrated Circuits Text*; *Safety First Manual*; and *Chip Packaging Manual*. His books and training materials are used by chip manufacturers, industry suppliers, colleges, and universities. Peter Van Zant Associates' customers include Intel, National Semiconductor, Applied Materials, Air Products and Chemicals, SCP Global Inc., and a number of educational institutions. Mr. Van Zant is also the elected District 1 Supervisor in his home county of Nevada in California.

vacuum A low-pressure condition.

vapor phase epitaxy (VPE) An epitaxial deposition system that can combine several source gases to deposit compound semiconductors.

vapor priming A technique in which primer is applied in a vapor state such that the wafer never comes in contact with any possible contamination in the liquid or, in the case of HMDS, any particles of hydrolyzed HMDS.

via Vertical opening filled with conducting material used to connect circuits on various layers of a device to one another and to the semiconducting substrate; serves same purpose as "contacts."

viscosity The qualitative measure of liquid flow. Viscosity measurements are made by measuring the force required to move an object through the liquid. It is a measurement of "internal friction."

VLF hood A workstation with vertical laminar airflow to keep particulate levels low.

VLSI (very-large-scale integration) Refers to chips with between 100,000 and 1,000,000 components.

volatile memory circuit A memory circuit that loses its data when power to the chip is lost.

voltage The force applied between two points causing charged particles (and hence current) to flow.

wafer A thin, usually round, slice of a semiconductor material from which chips are made.

wafer fabrication The series of manufacturing operations in which the circuit or device is put in and on the wafer.

wafer flat Flat area(s) ground onto the wafer's edges to indicate the crystal orientation of the wafer structure and the dopant type.

wafer sort The step after wafer fabrication during which the electrical parameters of integrated circuits are tested for functionality. Probes contact the pads of the circuit to conduct the test, leading to the name "prober" for the equipment that performs electrical tests on each die site of completed wafers.

wafer sort yield The number of functioning die at wafer sort as compared to the total number of die started; typically, the lowest major yield point for integrated circuits.

wire bonding An assembly step in which thin gold or aluminum wires are attached between the die bonding pads and the lead connections in the package.

X-ray aligner An aligner tool that uses X-rays and a mask to expose resist-coated wafers.

X-ray exposure system Imaging system using X-rays as the exposure source. Due to their short wavelengths, X-rays exhibit no detrimental diffraction effects.

PRINTED WIRING BOARD TECHNOLOGY

Printed wiring boards (*PWB*) have been in commercial use since World War II; however, related concepts originated 40 years prior to their commercialization. The founder of Sprague Electric, while still an apprentice, had the idea in 1904 of eliminating point-to-point wiring. When he conferred with his mentor on how to implement this new concept, his mentor suggested that silver reduction, as used in mirror manufacture, or the printing of graphite pastes on linen paper, might prove to be suitable. Sprague's mentor was Thomas Edison.

It was not until 1936 that modern printed boards were conceived of by Paul Eisler in England. Toward the end of World War II, a technology developed by the US National Bureau of Standards (*NBS*) was used in volume production of US Army VT proximity fuses for rockets and mortars. The production technology used was not the "print and etch" technique of Eisler, but rather printed silver paste conductors and graphite resistors screen printed onto ceramic substrate, using techniques more commonly associated with today's hybrid industry. It was this technique that ushered in commercial use of printed circuits. After World War II, the demand for consumer products of all types, particularly electronic for radio and early television industries, expanded at a tremendous rate.

Since the origin of *PWBs*, their evolution toward increasing complexity has generally been quite orderly. After reaching maximum density (based on contemporary fabrication limitations), single-sided boards were replaced by double-sided boards, which allowed wires to cross over each other without shorting and without the need for adding special jumpers. This was accomplished first by "Z" wires, then by eyelets, and finally by plated-through holes (*PTHs*). Figure 1 shows this Z-Axis interconnection evolution.

PWB Technology

Printed wiring boards are sometimes referred to as the baseline in electronic packaging. Electronic packaging is fundamentally an interconnection technology and the *PWB* is the baseline building block of this technology. It serves a wide variety of functions. Foremost it contains the wiring required to interconnect the component electrically and acts as the primary structure to support those components. In some cases it is also used to conduct away heat generated by the components. The *PWB* is the interconnection medium upon which electronic components are formed into electronic systems.

The constant pressures for improvements in *PWB* technology arise in all aspects of this technology. Electrically, the increase of high-speed and high-frequency electronic systems creates demand for *PWBs* having lower electrical losses. In addition, higher operating voltages increasingly require *PWBs* with greater resistance to voltage breakdown, high-voltage tracking, and corona. Aside from the requirements for higher electrical performance of *PWBs*, higher electronic system functional densities and the resultant higher thermal densities create demand for lower thermal resistance of *PWB* materials.

New developments in component technology in the 1960s and 1970s, with the movement away from through-hole technology to the higher density surface mount technology (*SMT*), have forced innovations in *PWB* materials and processes. The constant trend toward higher-functionality integrated-circuit (*IC*) components

2 PRINTED WIRING BOARD TECHNOLOGY

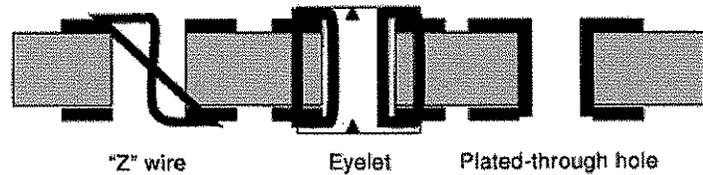


Fig. 1. Z-Axis interconnection evolution.

with higher input-output (I/O) pin counts of the IC packages has resulted in increased demand for fine-feature PWBs. Experts once predicted the demise of the PWB, believing that the increasing degree of integration in semiconductor chips could make the PWB unnecessary. However, increased integration in semiconductors has only served to make the PWBs more complex and more indispensable than ever.

Printed Wiring Board System Types

Printed wiring boards can be classified into several categories based on their dielectric material or their fabrication technique. PWBs can be classified into two basic categories based on their fabrication technique: *graphical* and *discrete-wire* interconnection boards: "Graphical" interconnection board is another term for the standard PWB, in which the image of the master circuit patterns is formed photographically on a photosensitive material such as glass plate or film. The image is then transferred to the circuit board by screening or photoprinting the artworks generated from the master. Discrete-wire interconnection does not involve an imaging process for the formation of signal connections. Rather, conductors are formed directly onto the wiring board with insulated copper wire. Figure 2 shows the detailed classification of PWB technologies.

Graphically Produced Boards

The majority of current PWBs are graphically produced. Graphically produced boards can be classified into two categories based on the dielectric material: *organic* and *ceramic* printed wiring boards.

Organic PWBs. These PWBs are fabricated using an organic dielectric material with copper usually forming the conductive paths. Organic-based boards can be subdivided into the following classifications: rigid, flexible, rigid-flex (combining the attributes of both rigid and flexible boards in one unit), and molded. Each of these classifications, except for molded, can be further subdivided into single-sided (*SSB*), double sided (*DSB*), multilayer (*MLB*), or high-density interconnect structure (*HDIS*) printed wiring boards.

The circuit interconnection pattern can be created by two techniques: subtractive or additive. Subtractive metalization of the printed wiring board involves imaging the conductor pattern on copper foils using a photoresist material and one of two image-transfer techniques—screen printing or photo imaging. The resist acts as a protective cover defining the conductor patterns while unwanted copper is etched away. Additive metalization involves chemically plating the conductors on top of the dielectric material.

These metalization techniques can be used with a variety of dielectric materials to achieve various mechanical and electrical characteristics in the final product. Among the most common dielectric materials are epoxy/*e-glass* (electronic grade glass), laminates used in the fabrication of rigid PWBs, and polyimide film used in the fabrication of flexible printed wiring boards. The rigid-flex boards use a combination of these two materials. Molded PWBs use high-temperature thermoplastic resins.

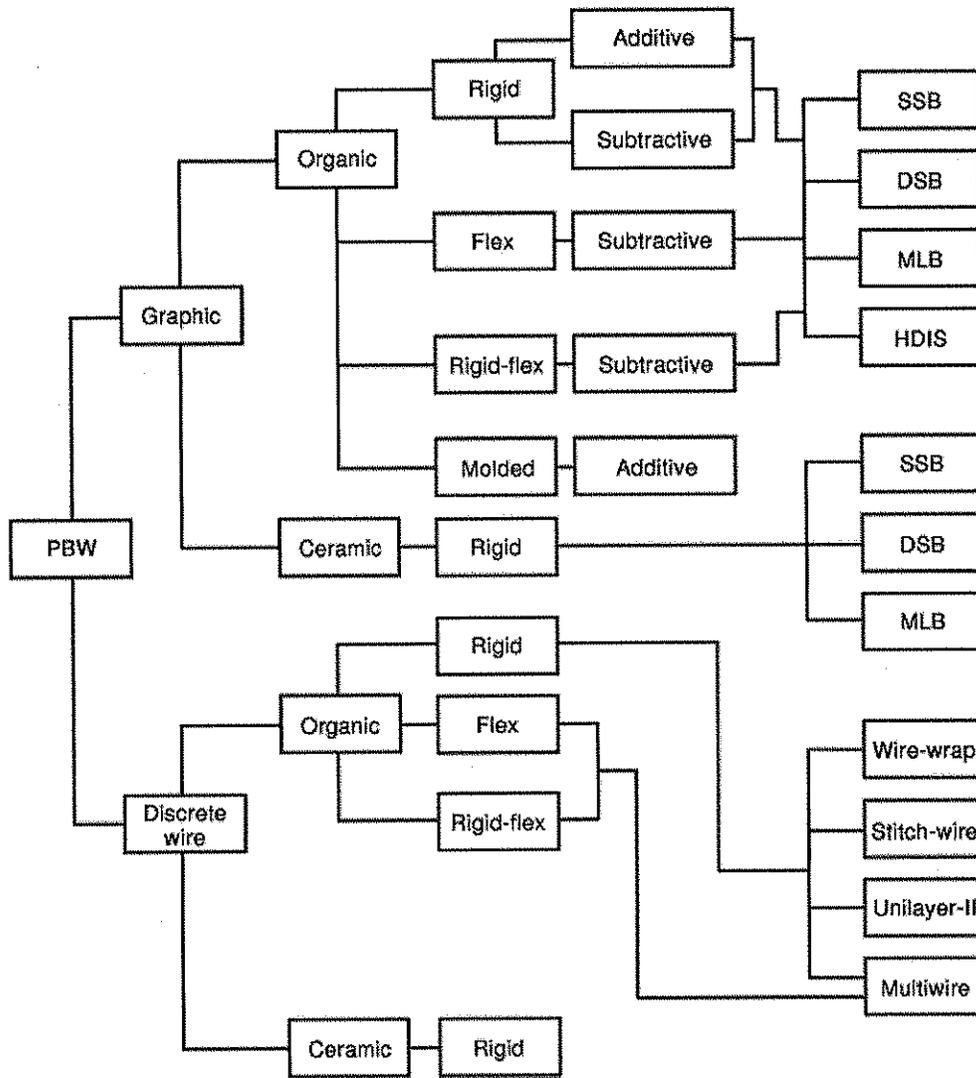


Fig. 2. Detailed classification of printed wiring boards.

Rigid PWBs. The rigid PWB is fabricated from copper-clad dielectric materials. The dielectric consists of an organic resin reinforced with fibers. The most commonly used fiber materials are paper and e-glass. Quartz, aramid, and S2-glass are other fibers which have been used in specialized advanced packaging as well as high-speed applications. The fibers are either chopped (usually paper) or woven into fabric (glass). The organic media can be of a wide formulation and include flame-retardant phenolic, epoxy, polyfunctional epoxy, or polyimide resins. Built within the laminate structure may be low coefficient of thermal expansion (CTE)-clad metals such as copper-invar-copper (CIC) or copper-molybdenum-copper (CMC) for decreasing the CTE of the overall PWB structure.

4 PRINTED WIRING BOARD TECHNOLOGY

As the name implies, rigid PWBs consist of layers of the organic laminates that are laminated through heat and pressure into a rigid interconnection structure. This structure is usually sufficiently rigid in nature to be able to support the components that are mounted to it. Specialized applications may require the PWB to be mounted to a support structure. The support structure may be used to remove heat generated by the components, decrease the movement of the PWB under extreme vibration, or decrease the CTE of the PWB in surface-mount technology (SMT) applications.

The rigid PWB interconnection structures may be further subdivided by the number of wiring layers contained within the structure and the fabrication of these layers into four categories—single-sided board (SSB), double-sided board (DSB), multilayer board (MLB), and high-density interconnect structure (HDIS). Figure 3 shows a cross-sectional view of each type.

Single-Sided PWB. A single-sided PWB consists of a single layer of copper interconnection on the component side of the PWB. The rigid dielectric material is fabricated from multiple layers of unclad laminate material pressed to the final end-use thickness. A single layer of copper cladding is applied to one of the outside layers during this process. In some instances double-sided copper cladding may be used, with the copper on one face being completely etched away during processing.

The base laminate of single-sided boards can be of woven or paper (unwoven) materials with copper foil, usually of 1 oz. or 2 oz. weight, clad to one side. It should be noted that copper cladding is most often referred to by its weight (1 oz/sq.ft. equals 0.00137 in. thickness) rather than by its thickness. The raw clad laminate is first cut into working panels suited to the equipment, which will handle the subsequent operations. The panel is then drilled or punched to provide a registration system. Laminate flatness is important in achieving a good registration baseline. This is critical in an automated print and etch system because the panel tends to warp after the copper is removed during etching. This warping allows stresses built into the material during its fabrication to be relieved. Excessively warped panels may not register properly for subsequent operations.

The individual artworks that define the conductor patterns are then arranged or panelized so that one or more PWBs will be produced from a single panel. This is accomplished by stepping and repeating the patterns into a panel phototool. Once the panel layout is established, the panel can be drilled or punched to produce the final hole pattern. Holes required are either drilled in glass-reinforced products or punched in paper-reinforced products. Registration of the conductor pattern to holes is accomplished through either the right-angle edge of the panel or on pilot holes contained in opposite corners of the panel. Drilling of holes is usually done after the panels are first cut; punching of holes is done as the last operation.

Following the drilling operation, the etch resist is applied and the circuit pattern formed. This pattern can be made by printing a liquid resist or photo imaging of a film or liquid. The next step is to etch away the unwanted copper from the laminate, leaving only the desired circuit pattern. Finally the resist is stripped and the single-sided board is complete in panel form. At this point additional processes such as plating or solder masks may be performed, or the individual boards may be sheared or routed from the panel.

While single-sided boards with their simplicity might be doomed due to the increased complexity of modern electronics, they continue to have a small market, especially where cost is a strong driver.

Double-sided PWBs. From a historical perspective the double-sided board is probably the most often designed type of all PWBs. It retains much of the production simplicity of the single-sided board but allows circuit complexities far in excess of 2:1 over its simpler cousin. This is the case because it allows basic *x* and *y* routing of the circuit on its two outer faces, thus improving the routing efficiency and the circuit density.

Interconnection of the two conductor patterns is accomplished through drilling and subsequent plating or filling the interconnection holes, called vias. The most widely used method is to plate the vias with copper.

Double-sided boards are fabricated from laminates with copper clad on both outside layers. The copper may be clad to a variety of dielectric materials. The material is usually purchased from a laminator who specializes in providing laminates to the electronic industry.

One the raw laminate is cut into panels, the fabrication process begins with the interconnection hole drilling. The via holes may also serve as mounting holes for the components. After the via hole pattern has

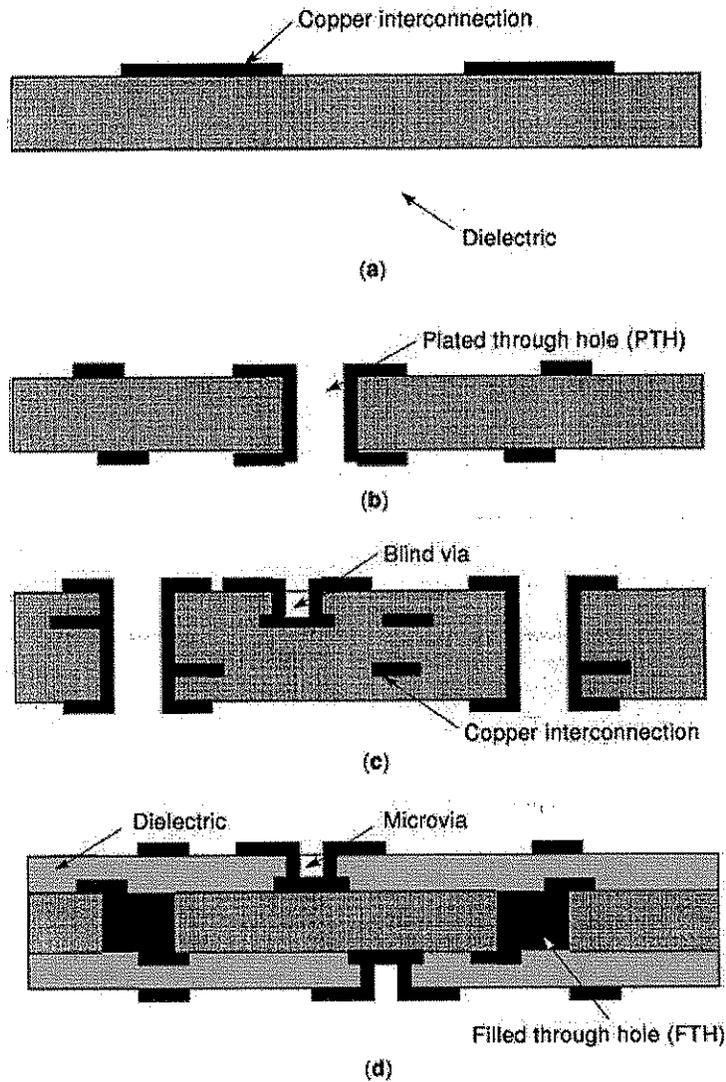


Fig. 3. Cross-sectional views of organic PWBs.

been drilled, the holes may be filled with the conductive ink or the panel is copper plated by an electroless technique in preparation for subsequent plating by either of two methods—pattern plating or panel plating.

The conductor image is formed in a similar way as with single-sided boards, except that the photoresist application and imaging take place on both sides of the panel. Obviously, the registration of the photo images from one side of the panel to the other is critical. The circuit pattern on one side must be properly registered to the pattern on the other side, or the plated through hole (PTH) will not properly connect between the two sides. The next step is to etch away the copper laminate, leaving only the desired circuit pattern. At this point

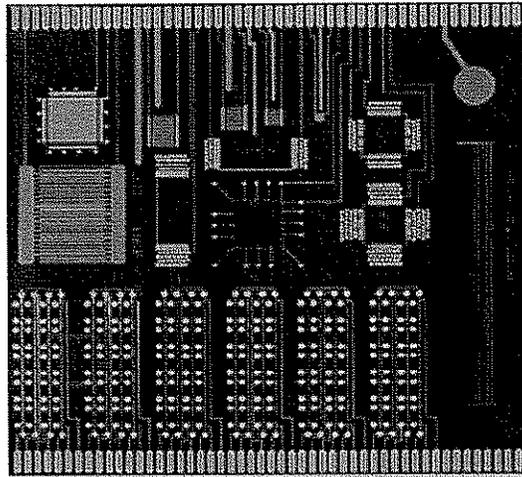


Fig. 4. Typical rigid multilayer PWB (Courtesy Motorola Inc.).

additional processes such as resist stripping, plating, or solder masks may be performed and the individual PWBs then are sheared or routed from the panel.

Multilayer PWBs. Multilayer boards are those PWBs having three or more conductive layers, including and pads-only layers. The typical modern multilayer board will have anywhere from 4 to 12 layers of circuitry, with some specialized application requiring upward of 50 layers. Most multilayer boards are fabricated by laminating single- or double-clad, patterned sheets of thin laminate together using partially cured resin (known as B-stage) in a carrier fabric. The single- or double-clad laminate material is processed similarly to the single- or double-sided PWB, except that the via or component holes are usually not drilled until after lamination. It should be noted here that the importance of registration is amplified as the layer count increases. Increased pad sizes may be required to minimize via hole breakout due to misregistration. The same requirement may limit the size of panels due to run out of the circuit features. Following the fabrication of the individual layers or layer pair, a "book" of layers and their interposed B-stage bonding layers are stacked together in a particular sequence to achieve the required lay-up. This book is laminated under heat and pressure to the appropriate thickness for the final board. The outer layers are not pre-etched so that the laminate book appears the same as a double-sided copper-clad laminate of comparable thickness. After lamination the book is processed the same as a thick double-sided board. The book is drilled to add the via holes and then processed as if it were a double-sided board using plated through holes.

In some cases standardized layers, such as power or ground distribution, can be "mass laminated" into the raw laminate. This is a very cost-effective means of achieving multilayer density at near double-sided board cost since the outer layer processing and via drilling is identical to that for double-sided PWB processing. Where circuit density requirements cannot be achieved with through hole multilayer boards, techniques such as blind or buried vias are used to increase the interconnection wiring density on a given layer. Where these techniques are used, the inner layer pairs are fabricated as double-sided boards, complete with plated vias, and then assembled into books for processing into multilayer boards. Thus the inner layer may be interconnected by holes through the entire board. Similarly, blind vias may connect to the first or subsequent buried layer on each side of the board without penetrating the entire board. The multilayer board has achieved a cost and reliability level that allows its use in any level of electronics. It is often seen even in toys. Figure 4 shows a typical rigid multilayer PWB.

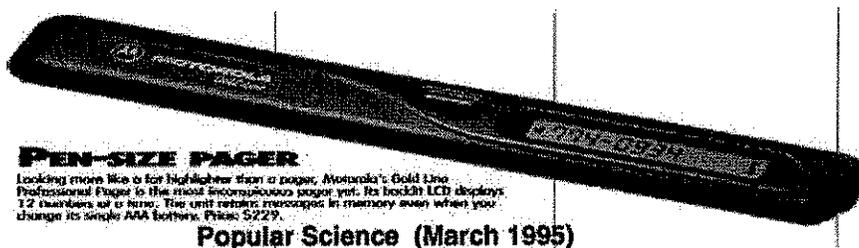


Fig. 5. Goldline Pen Pager (Courtesy Motorola Inc.).

High-density Interconnect Structures. The printed wiring board (PWB) industry is driven by frequent improvements in technology, reduction in cost, and increasing performance demands on material and process control. High-density interconnect structures PWB technology is a recent area of investigation that is rapidly accelerating in activity at the most advanced companies.

As shown in Fig. 5, new electronic products are required to be smaller, faster, lighter, and cheaper in order to compete in today's market. In order to achieve these requirements, fine pitch area array packaging, fine pitch BGA, and flip chip on board assembly technologies are being implemented. The rate these packaging technologies can be adopted, is largely being dictated by the availability of higher density PWB technologies with significant reduction in conductor lines width, and via size at relatively lower cost.

The two disturbing trends creating the need for high-density interconnect structures (HDIS) are the increased number of through holes and blind vias in the consumer electronic products and the dramatic increase in the cost of drilling smaller diameter vias. Drilled holes and vias are among the basic structures of PWBs; however, they have significant problems. For example, since the via and pad can block routing channels, each year the via and pad get smaller. Standard PWB technology can produce a via pad size of 0.020 in. with a 0.0125 in. to 0.010 in. drilled hole. These holes can decrease to 0.008 in., but as they get smaller, they also get more expensive. As a result, small hole drilling can contribute as much as 30% to 40% of the total cost of the PWB. Currently, the single highest cost associated with fabricating a leading-edge blind-and-buried PWB is drilling cost. Also, as the holes get smaller for the same thickness board, the aspect ratio increases. This tends to decrease reliability, as high-aspect holes have problems getting sufficient plating solution and solder into the hole.

The real benefit of HDI is in the small holes, identified as "microvias." These holes are very small, defined by the Institute for Interconnecting and Packaging Electronic Circuits (IPC), as equal to or less than 150 μm (or 0.006 in.). Currently there are three major HDI technology classes that address the future market needs. In many implementations, these HDI layers are constructed as the outer layers on a standard double-sided or multilayer PWB, using a thin, nonreinforced resin as the dielectric. The HDI dielectric has thickness of 0.0015 in. to 0.003 in. Vias are created by photoimaging, laser ablation, or plasma etching.

Materials used for HDI structures are different from those used to manufacture standard PWBs. There is a similarity in the dielectric properties, yet the HDI thin materials are coordinated with the process used to produce microvias. Some materials are laminated to a core structure; others are deposited. If the method for microvia fabrication uses photosensitive techniques, then the dielectric will contain a photopolymer. Fabrication of HDI structures requires that these thin materials be deposited on a core. The core may be passive, like a sheet of aluminum, or an active part of the circuit, like a multilayer PWB. Figure 6 shows a cross-section of an HDI structure deposited on a multilayer core. A brief description of the main HDI via forming technologies is shown in Fig. 7.

The process steps shown in Fig. 7 can be repeated on both sides of the core to build more circuit layers. The maximum number of layers that can be added is limited by yield, cost, and routing capability.

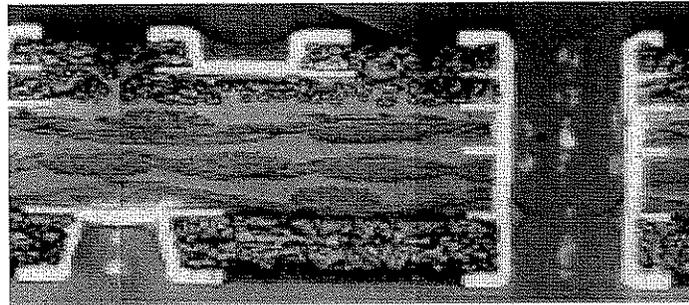


Fig. 6. Cross-sectional view of HDI structure on a multilayer core.

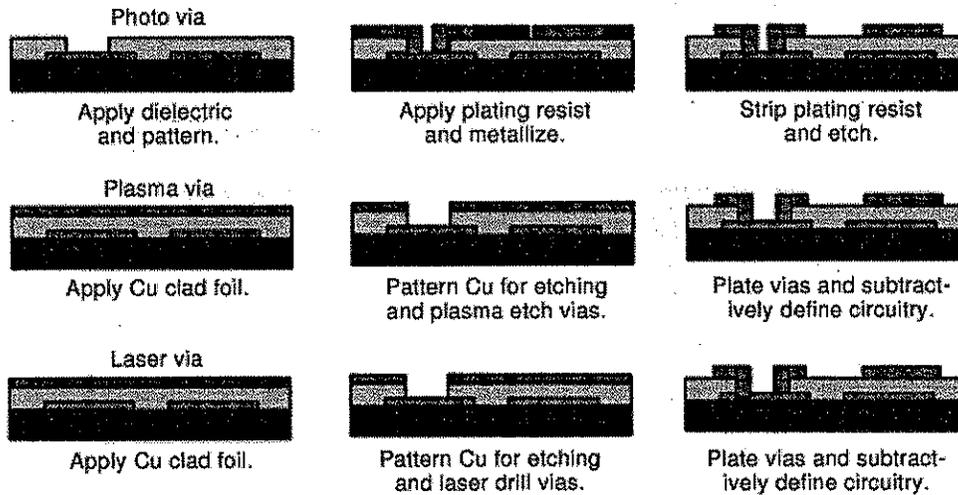


Fig. 7. HDI structure technology classes.

Photovia. The photovia approach is based on a photoimaged dielectric, usually a resin, and pattern plating to form the via and circuitry connections. IBM developed the first photovia process, called surface laminar circuitry (SLC). The different photovia approaches can typically be broken down into three categories determined by the metalization process: (1) panel plate, (2) pattern plate, and (3) full build pattern plate. Figure 5 shows a typical process flow used for pattern plate photovia technologies. This process flow is typical of the majority of photovia technologies available. IBM was the initial developer of the photovia technology.

Plasma Etching. Plasma-etched vias rely on the use of copper-clad nonglass-reinforced laminate, such as polyimide or epoxy resin coated copper (RCC) for the dielectric. Plasma is used to etch the dielectric and form the microvias. The copper foil is used as a conformal mask to define the via openings as seen in the process in Fig. 5. Dyconex developed the plasma etching process.

Laser Ablation. Laser-ablated vias currently rely on the use of nonglass-reinforced laminate, such as aramid or resin coated copper for the dielectric. There are three different drilling options for forming the microvias: (1) TEA-CO₂ (transverse excitation in atmospheric pressure), Excimer laser, and Nd:YAG (neodymium:yttrium-aluminum garnet). Major strides are being made in the industry to improve the throughput of the lasers to make the cost more competitive with mass generation techniques such as photo and plasma

technologies. The laser process shown in Fig. 5 uses the TEA-CO₂ laser with conformal copper mask approach for defining the microvias. The Nd:YAG laser ablates copper and the organic dielectric.

Flexible Printed Wiring. As defined by the IPC, flexible printed wiring is random arrangement of printed wiring, utilizing flexible base material with or without cover layers. Interconnection systems consisting of flat cables, collated cable, ribbon cable, and sometimes wiring harnesses are sometimes confused with flexible printed wiring. Flexible printed wiring is used in applications requiring continuous or periodic movement of the circuit as part of the end-product function and in those applications where the wiring cannot be planar and is moved only for servicing. Visually, flexible printed wiring looks similar to rigid printed wiring. The main difference in the products is the base or dielectric material. Flexible printed wiring is manufactured using ductile copper foil bonded to thin, flexible dielectrics. The dielectric substrate is the base film on which the printed conductors are fabricated. The dielectric insulates conductors from each other and provides much of the mechanical strength of the circuit. The choice of a flexible rather than a rigid dielectric is the main characteristic that distinguishes flexible printed wiring from rigid printed wiring boards. In addition to the typical electrical and mechanical properties, the dielectric substrates have considerable influence on dimensional stability and flexibility of the flexible circuitry. Some of the most common dielectric materials used include polyimide (*Kapton*), polyester terephthalate (*Mylar*), random fiber aramid (*Normex*), polyamide-imide Teflon TFE and FEP, and polyvinyl chloride (*PVC*). As with rigid PWBs, flexible printed may be manufactured in single-sided, double-sided, or multilayer configuration. The conductor patterns are formed in a manner similar to rigid PWBs, using either screen printing or photo imaging of a resist to form the conductor pattern and then etching the unwanted copper. A variety of adhesive materials are used in their manufacture to bond the various layers together. Typical adhesive systems include polyester, epoxy/modified epoxy, acrylic, phenolics, polyimide, and fluorocarbons. The properties of an adhesive must be compatible with those of the dielectric substrate: Adhesives must be capable of withstanding the processing conditions and chemicals used in printed wiring manufacture without delamination or degradation of properties. Flexible circuits generally have higher non-recurring costs and lower recurring costs than other wiring methods. Flexible wiring are, therefore, generally less cost competitive at very low production volumes and more cost effective at high production volumes.

Due to the extreme flimsiness of flexible wiring, when components are to be mounted, adequate reinforcement must be added to the flexible wiring to eliminate stress points at the component-circuit interfaces. Reinforcements typically used are simple pieces of unclad rigid laminates or complex formed, cast, or machined metals or plastics to which the flexible wiring is laminated.

Rigid-Flexible PWBs. This PWB consists of single or multiple flexible printed-wiring plies integrated into rigid PWBs and interconnected through plated-through holes. Most often the flexible wiring forms the innermost layers of the rigid PWB and its flexible appendages emerge from the rigid section of the board to form flexible terminations or other rigid-flexible composites. The rigid-flexible wiring exhibits the lowest profile form factor of all the interconnect system types. The benefits of rigid-flex wiring are apparent in the design, manufacturing, insulation and assembly, and product enhancement of the end-product. The designer has increased conceptual freedom in the end-product design. Conformability, three-dimensional interconnects, and a space-saving form factor are benefits. In many cases reduced interconnect length leads to optimal electrical performance. Mechanical and electrical interfaces are reduced, and mechanical, thermal, and electrical characteristics are more repeatable than with conventionally wired systems.

In manufacturing their use leads to reduced assembly costs within a totally utilized interconnect system. There are increased opportunities for automation. In addition, reduced system interconnect errors and improved system interconnect yields occur.

Molded PWBs. One other PWB concept with many functional and design advantages in many application areas is the molded or three-dimensional PWB. These boards are usually nonplanar (three-dimensional) and consist of conductive materials selectively applied to either extruded or injection molded thermoplastics resins. Standard rigid PWB laminate structures produce formed circuitry only in two dimensions, by comparison. Representative molded three-dimensional circuits might be cases or covers which contain an electronic

assembly, or molded three-dimensional IC chip carrier. This technique can be applied to any three-dimensional molded part onto which formed circuitry is beneficial. A single three-dimensional case with integral formed circuitry, for instance, could replace a two-part case and separate circuit board assembly. High-temperature thermoplastics are commonly used for in these applications due to the soldering of parts to the circuitry formed on them. The most common used materials are polyethersulfone, polyetherimide, polyphenylene sulfides, and various polyesters. Each resin has its own unique set of properties which must be matched to the functional and cost requirements of the end product. The benefits of using this technology in a functional part are many and varied. The resin system's thermal and electrical properties are superior to standard epoxy/e-glass rigid laminate materials. Manufacturing tolerance of the finished part can be held to ± 0.001 in. Holes can be rectangular, square, oval, or tapered. Features such as connectors, clips, bosses, and spacers can be molded into the finished part. The formed three-dimensional circuitry can be applied in several ways, with the most common application methods being circuitry transfer process and two-step molding process. In the circuitry transfer process, the molded part is made as one step, and the circuitry pattern is applied to a flat release sheet in another step. The pattern is applied by screen printing of a polymer thick-film material onto the release sheet. A polymer thick film as used here is basically a conductive powder such as copper or silver mixed into a polymer resin to a screenable form. The release film is slit, punched, and so on, where required, so that it can be inverted onto the molded form in a contour that fits the contour of the molded part exactly. The circuit pattern is now pressed, or transferred from the release sheet onto the three-dimensional contour of the molded part. This is done in a heated press in order to thoroughly bond the cured polymer thick-film circuitry to the molded part. The "Konec" processes, developed by Amoco Performance Products, use polymer thick films to manufacture molded interconnect. The two-step molding process is performed by overmolding a separate initially molded part. This process usually involves the selective additive plating of copper to form the interconnect. In this process, the initially molded part (the first step of molding) is molded using a plastic material which is catalyzed so that it becomes a platable plastic. The platable plastic part is molded so that any ink or contact area that is to become circuitry protrudes from the rest of the molded part. This first molding of platable plastic is now placed in a second mold of the final desired part form, but with the protruding final circuitry areas contacting the mold walls. Thus in this second molding step, the final part is molded with an uncatalyzed, hence unplatable, plastic. When this piece is removed from the mold, the areas of catalyzed plastic are exposed at the surfaces. Plating of the part will then plate only the catalyzed plastic surfaces. This forms the circuitry pattern. The rest of the part will not be plated.

Ceramic PWBs. These PWBs are classified by their method of manufacture and type of metallization. There are four distinct types: (1) *Thick films*, which use alumina, beryllia, and similar materials as the substrate base material and fired thick-film dielectric paste as the dielectric. Conductors are formed from fired conductive noble metal pastes. (2) *Thin films*, which use ceramic, glass, quartz, silicon, or sapphire as the substrate base and deposit various metals by plating, sputtering, or vapor deposition. (3) *Cofired* substrates can be broken into two distinct grouping. Cofired ceramic uses ceramic tape as the dielectric that is cofired with refractory metal pastes which form the conductors; cofired low-temperature tape uses a glass/ceramic tape dielectric which is cofired with noble metal pastes which form the conductors. (4) *Direct-bond copper*, which directly bonds copper conductors to a ceramic substrate. All of these ceramic-based PWBs are most often referred to as substrates. Ceramic boards do offer advantages, compared to organic boards. The ceramic dielectric is inherently much more rigid than organic material dielectrics. Flatness values of 0.002 in./in. to 0.003 in./in. are normal and can be as low as 0.001 in./in. Component soldering (183° to 240°C) is usually performed above or near the glass transition temperature T_g of organic materials (100° to 240°C) and can lead to damaged PWBs when process is controlled improperly. Higher thermal conductivities available with ceramic materials offer improved thermal management over organic boards. When thermal vias are required, the smaller buried vias available with ceramic boards provide a low thermal resistance while sacrificing less routing area. The coefficient of thermal expansion (CTE) matching to hermetic component cases is available with a ceramic board and offer improved solder joint reliability in surface mount technology (SMT) applications. Increased costs and design time are

disadvantages to the use of ceramic boards. A weight penalty is usually paid when ceramic boards are used. The ceramic and noble metal materials used in ceramic boards are also more costly than their organic counterparts. The demand for ceramic boards has usually been in low-volume military and avionics applications. This has led to limited number of ceramic PWB fabricators, which has caused costs to remain high.

Thick Film. This class of ceramic PWBs is manufactured by building up alternating layers of conductors and dielectric on a ceramic substrate. A thick-film substrate may be called a true printed circuit in that resistive elements may also be built into the substrate. Thick-film substrates have dielectric thickness of 0.0015 in. to 0.0025 in. Each layer is pattern-printed onto the substrate using screen or stencil printing process.

Several different ceramic materials can be used as the substrate base. These include alumina, beryllia, aluminum nitride, boron nitride, silicon carbide, and silicon nitride. Dielectric, conductor, and resistive inks (pastes) are printed and fired to build the interconnect structure.

The manufacture of a thick-film ceramic PWB begins with the generation of artwork defining the following: conductor patterns, dielectric layers including via openings in multilayer applications, via fill patterns, and resistor artworks when required. From this artwork a screen or stencil for each wiring, via, resistor, and dielectric layer is developed. A photosensitive polyvinyl, or polyimide emulsion is next applied to the screen, and the conductor, dielectric, via, or resistor pattern is photoimaged on the emulsion under ultraviolet light using the artwork. Stencil printing involves etching the patterns to be printed in a thin metal foil, usually nickel or brass. This once again uses photosensitive materials as a photoimaging operation to define the pattern and then etching away the unwanted metal similar to etching copper on a PWB laminate. The metal stencil is then mounted in a metal frame. The advantages of stencil over screen meshes are many. They offer more uniform print thickness, greater resolution, reduced dimensioning capabilities, and easier process control. The ceramic substrate is prepared by cutting to size using laser drilling, diamond scribing, or ultrasonic milling. The laser is by far the most prevalent method. Overlapping of the laser drill hole pattern can yield a smooth cut surface. Spacing of the holes yields a perforated surface, which can be used to define a number of substrates on a single ceramic panel. This "snapstrate" can be processed, and after the processing is completed, the individual substrates can be snapped along the perforation. Following substrate cleaning, the metallization process begins. Conductive, dielectric, or resistive inks contain the desired metals or conductors. These are combined with glass frits to allow bonding during firing and needed solvents to accomplish a definable print. Each layer is printed, dried to volatilize the solvents, and then fired in a furnace. This print, dry, fire sequence continues until the multilayer structure is complete.

Thin Film. Thin-film ceramic boards are normally limited to specialized designs or single-layer applications. They are more expensive and difficult to multilayer when compared to thick-film substrates. Their use requires the substrate surface to be very flat and smooth and causes higher-purity ceramics to be used. These include alumina, glass, quartz, silicon, or sapphire. Thin-film metallization uses noble metals (such as gold) and are used most often in microwave applications due to their improved electrical performance over thick-film substrates at higher frequencies. Thin-film interconnections in multilayer applications are accomplished through buried vias, as is the case with all ceramic PWBs. The top and bottom metallization on a double-sided substrate can be connected using plated-through holes for electrical interconnection or improved thermal performance. Metallization patterning of thin-film ceramics is accomplished through the use of photo lithography, plating, etching, vapor deposition, and sputtering methods.

Cofired. This type of ceramic PWB requires the printing of pastes containing conductor metallization onto unfired tape (dielectric) materials. These layers are then stacked and cofired together in a furnace to form the interconnect structure. The unfired tape materials can be either ceramic or a low-temperature dielectric. The ceramic tape system requires higher firing temperatures. This results in refractory metals such as tungsten, molybdenum, or tungsten copper to be used as the conductor within the paste. These metals have higher vaporization temperatures to withstand the firing, but lower thermal and electrical conductivities than the noble metals (gold, silver, and copper). Their lower conductivities typically limit the use of these substrates to digital applications. The conductor paste is applied to the tape using a screen or stencil similar to the thick-film

process. For multilayer applications, holes are punched in the dielectric prior to printing. The conductive paste fills the holes and later forms a buried via during the firing operation. After all layers have been printed, they are stacked in the proper sequence, laminated together under heat and pressure, and fired to solidify the ceramic. Upon completion of the cofiring operation, the exposed refractory metals are electroplated with typically 0.00008 in. to 0.00035 in. of nickel and 0.00005 in. to 0.0001 in. of gold. The nickel acts as a barrier to intermetallic formations between the gold and tungsten and as a corrosion barrier. The gold serves as a wire-bondable or solderable surface for component attachment. The dielectric tape systems are composed of lower-temperature reflow glasses similar to those found in thick-film pastes. The printing, stacking, and laminating operations are the same as those used for ceramic materials. The firing, however, occurs at lower temperature, which allows the use of noble metal addition, no additional platings are required upon postfiring.

Cofired PWBs offer distinct advantages over thin- or thick-film processed PWBs. Multilayering is limited only by the thickness limitation of the overall package. Each fired layer is 0.003 in. to 0.012 in. thick, depending on the tape thickness used. Thermal vias may be more readily incorporated into the design using an array of vias punched in the dielectric and filled with conductive pastes. Cutting of the tape prior to stacking and firing can allow cavities to be formed in the final product to allow component mounting. The main disadvantages are in the longer life-cycle time needed to develop the tooling required to produce the item.

Direct-Bonded Copper. As the name implies, a direct-bonded copper board uses copper directly bonded to a ceramic dielectric. The most commonly used ceramic is alumina. The direct-bonded copper structure offers improved thermal and structural performance compared with conventional thick- or thin-film technologies using alumina dielectric. The process involves oxidation of the surface of a copper foil, which is then placed against a ceramic substrate. The pieces are placed in a furnace which reflows the copper oxide and fuses it with the surface ceramic oxides. This process directly bond the two materials together. The bonding process occurs at approximately 1000°C. During cooling, the copper contracts at a much higher rate than the ceramic due to its greater CTE. The cooling increases the tensile strength of the ceramic by an order of magnitude by placing it in compression. This allows thinner ceramic materials to be used and will decrease the overall assembly height and reduce the thermal resistance of the board. The copper interconnect features can be formed by punching the copper sheet prior to attachment to the ceramic or by photoimaging techniques similar to those used in rigid PWBs after bonding to the ceramic. The latter process allows finer line features. Typically, 0.015 in. minimum line widths and spacings are used. Alternately stacking layers of copper and ceramic can create multilayer interconnect structures.

Discrete-Wired PWBs. Most discrete-wired boards use an organic rigid PWB as a base substrate, their primary difference being that the circuit is wired using discrete or individual wires. Wire-wrap and multiwire are the best known discrete-wire interconnection technologies. Because of the allowance of wire crossings, a single layer of wiring can match multiple conductor layers in the graphically produced boards, thus offering very high wiring density. However, the wiring process is sequential in nature and the productivity of discrete-wiring technology is not suitable for mass production. Despite thick weakness, discrete-wiring board are in use for some very high-density packaging applications.

Materials for Printed Wiring Boards

Printed wiring boards are designed in various sizes and shapes, use a variety of processes and materials, and perform a variety of electrical, mechanical, and sometimes thermal functions. Paramount to achieving a PWB that performs its intended function reliably, is producible, and is fabricated for the lowest cost possible, the designer must have a fundamental knowledge of the materials used in the end-product. However, the knowledge should not be limited to knowing the end-product material's electrical, mechanical, thermal, and chemical properties. Material knowledge should include environmental effects (thermal, mechanical, and humidity) on

properties and their impacts on the material's performance in the particular design. In addition, manufacturing-process-related stresses must also be considered.

Organic Rigid PWB Materials. Organic rigid PWBs consist of a dielectric material onto which is patterned some form of metallization, which creates the actual circuit. Fiber-reinforced resin dielectric materials, referred to as laminates, clad with copper sheets, are most commonly used for rigid PWB applications.

PWB Laminate. The laminate properties are related to the constituents in the composite laminated structure, that is, to the anatomy of the laminate. An organic rigid PWB laminate consists of three major elements and some auxiliary ones. The major elements are (1) the fabric, (2) the resin (which combined comprise the dielectric), and (3) the metal foil. The auxiliary elements are the adhesion promoters or treatments that are applied to the fabric and to the foil to assure maximum adhesion of the resin to the fabric and foil. The manufacture of a copper-clad PWB laminate begins in a machine called a *treater* or *coater*. Fundamentally, the operational sequence is that the fabric is fed off the fabric roll and through a dip pan containing resin. The resin-curing agent mixture in the dip pan is called A-stage, a term used to describe totally unreacted resin. The resin impregnates the fabric, is passed through a set of metering rollers (squeeze rollers) to control the thickness, and then passes through a treating oven for partial cure (polymerization) of the resin into the fabric. The oven is air-circulating or infrared and can be up to 120 ft. long. Most of the volatiles such as solvents in the resin are driven off in the oven. After the resin-soaked fabric is partially cured in the treater oven, the fabric-resin combination is called B-stage or prepreg. These two terms are used to describe the partially cured resin. Finally, the B-stage coated fabric is cut into predetermined sizes for laminating. The B-stage is especially critical since it can be undercured (understaged) or overcured (overstaged). Hence the B-stage must be closely controlled for optimum PWB laminates to be produced. Ideally, the B-stage will be dry to the touch and nontacky, but capable of reflow and optimized bonding in the laminating press. Two important factors in handling B-stage material are resin aging and moisture layers on the B-stage sheets. The resins used to impregnate the fabric are organic polymers. The nature of polymer reactions is such that resin curing, or polymerization, will slowly continue at all times, the reaction rate being a function of temperature. Therefore, since an optimum B-stage is only partially cured, the curing will continue toward overcure, especially in warm or hot conditions, such as summer shipping and storage. Under any given set of storage temperature conditions, a specific useful life, or shelf life, will exist for any given B-stage sheets. Thus cool shipment and storage conditions are usually recommended for B-stage stacks. The B-stage sheets must also be shipped and stored in dry conditions, since moisture film can be condensed onto cool sheets. When B-stage sheets with invisible moisture films are laminated together into a PWB laminate, moisture entrapment will result between layers in the cured laminate. During subsequent soldering operations on the PWB, this entrapped moisture will explode onto small entrapped delamination spots. These white spots, known as blisters, can be sufficiently large or dense to affect PWB performance and reliability. Figure 8 shows a delaminated PWB structure.

The final cured laminate is referred to as C-stage laminate and is achieved by pressure and heat in the laminating press. A final copper-clad C-stage laminate of a given thickness is made up of a number of thin B-stage laminates. This complete stack, including the copper foil, is pressed together and heated between flat plates, or platens, in a heated laminating press for the time required to completely polymerize the epoxy resin at the selected press temperature. Laminates used in the manufacture of single- or double-sided PWBs are usually thick laminates (>0.030 in.) and are made up of a number of thin unclad laminate B-stage plies. Multilayer PWBs use thin clad C-stage laminate plies bonded together with thin B-stage plies. Each ply thickness is typically in the 0.004 in. to 0.008 in. thick range.

Fabric Materials. There are four materials that usually constitute the base fabric of the PWB laminate, namely, paper, e-glass, quartz, and aramid fiber. A very common aramid material is manufactured by du Pont under the trade name Kevlar. Table 1 shows the properties of the various fabric materials. In some instances a hybrid mixture of these materials is used to achieve certain properties.

Paper-based materials are used with flame-retardant resins in low-cost PWBs, where laminate dimensional stability is not critical and where holes are punched in the material. Their use is mainly limited to

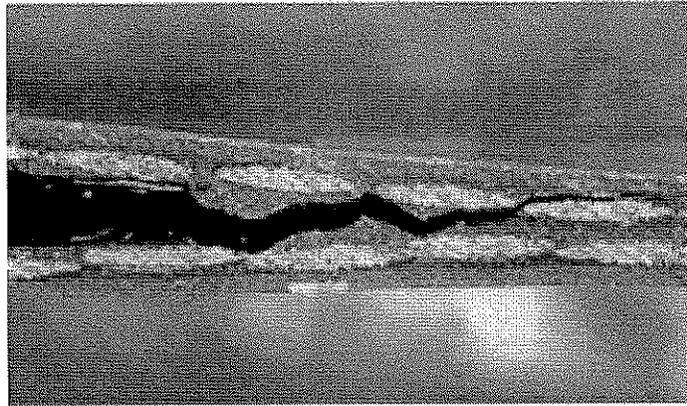


Fig. 8. Cross-sectional view of a delaminated organic rigid PWB.

Table 1. PWB Fabric Material Properties

	e-glass	Quartz	Aramid
Specific gravity, g/cm ³	2.54	2.20	1.40
Tensile strength, kg/mm	350	200	400
Young's modulus, kg/mm	7400	7450	13,000
Maximum elongation at 72°F, %	4.8	5.0	4.5
Specific heat, cal/(g·°C)	0.197	0.230	0.260
CTE, ppm/°C	5.0	0.54	-5.0
Dielectric constant at 1 MHz	5.8	3.5	4.0
Dissipation factor at 1 MHz	0.0011	0.0002	0.001
Thermal conductivity, W/(m·°C)	0.89	1.1	0.5

single- and double-sided laminates for consumer electronics such as toys, calculators, and radios. The most widely used material in PWB manufacturing is e-glass, a borosilicate type. Both randomly oriented glass-fiber mattes and woven glass-fiber fabrics are used. Its material properties satisfy the electrical and mechanical needs of most applications. Quartz and Kevlar-based fabrics have been used in PWB SMT applications. Their low CTE compared to that of e-glass along the fiber allows for a lower overall PWB CTE when processed with suitable resin. This is required in SMT applications to improve solder joint reliability. The raw material costs for these materials are higher than for e-glass. In addition, extra costs are incurred due to the difficulty in processing laminates made from these materials throughout the PWB fabrication cycle, especially drilling and laminating. Their applications have been mainly limited to high-reliability military and aerospace applications. Numerous types of base fabrics made from these materials are used, such as woven continuous fiber, short randomly oriented glass fibers known as glass mat, electrical-grade papers, and others. The woven continuous fiber fabric is the most common type used in PWB applications. Many fabrics, especially glass and Kevlar, do not bond well to the resins which are used to impregnate them. Thus to assure a strong laminate, it is necessary to treat the fabric with an adhesion-promotion treatment. Inadequate bonding of the fabric-resin

Table 2. Typical Resin System Physical Properties

Type	T_g , °C	Elastic Modulus 10^6 lb/in ²	Poisson's ratio	CTE ppm/°C	Thermal conductivity (Btu/in · ft · °F)	Dielectric constant at 1 MHz	Dissipation factor at 1 MHz
Epoxy	125	0.5	0.35	57.6	0.14	4.2	0.006
Polyimide	240	0.4	0.33	46.6	0.14	3.9	0.005
Cyanate ester	180	0.58	-	56.0	0.14	3.6	0.020
PTFE	-	0.05	0.46	99.0	0.14	2.1	0.0002

interface can result in the migration of water, plating solutions, copper etchants, and other liquids into the laminate during PWB fabrication processes.

Resin Systems. A wide range of resin materials are used in today's organic PWBs, with new formulations being brought to market continually. Most resin systems used in organic PWB laminates are a thermosetting plastic, with thermoplastic materials used primarily in microwave applications and in molded PWB applications. There are three resin systems used in laminates: (1) standard epoxies, (2) high-performance epoxies, and (3) polyimides. The most common resin used systems used are the standard epoxies. These are used in NEMA grade G-10 and FR-4 laminates and have a relatively low glass transition temperature T_g (105° to 125°C). T_g is the temperature at which a plastic changes from a rigid or harder material to a softer or glass-type material. It is a definite characteristic of all plastic materials, but not a property of the resin system where molecular bonds are broken. T_g is the point where the physical properties of the resin change due to a weakening of the resin system's molecular bonds. The G-10 epoxy is a general purpose bisphenol A difunctional epoxy, while the FR-4 epoxy is a brominated bisphenol A difunctional epoxy. The bromines make the FR-4 epoxy flame-retardant. These epoxies are easy to process and B-stage, and they have excellent adhesion to copper at room temperature. The high-performance epoxies are modifications of these difunctional epoxies, using smaller amounts of bismaleimide triazine (BT), polyimide, or tetrafunctional epoxy. They are made to increase the base epoxy resin T_g and improve the chemical and thermal stress resistance of the bisphenol A epoxies. The type of resin added and the percentage can cause T_g to vary between 125° and 200°C. Raising the epoxy resin T_g usually leads to resin system that is more brittle than the base epoxy. This can make the new resin more difficult to process and can lead to laminate reliability problems in harsh environments.

Polyimides are the third major type of resin system in use today for organic PWB laminates. The polyimide resins exhibit T_g values over 200°C. In addition to their higher T_g , they exhibit superior adhesion to copper at soldering temperature and have a lower CTE than epoxies. Their disadvantages are that they are quite brittle, and hence more care needs to be followed during their processing, they cost more, and they have a higher moisture absorption and a lower flammability rating. Modifications to polyimides are usually done with epoxies to improve their processability, reduce laminate moisture absorption, and improve their adhesion characteristics. To improve electrical performance (lower signal propagation delay) in high-speed applications, the laminate dielectric constant must be reduced. Though quartz and Kevlar fibers do have lower dielectric properties than e-glass, the lowering of the resin dielectric constant is the main driver. New materials have been developed, or are under development, to meet this challenge. Rogers Corporation has developed a family of lower dielectric constant laminates based on PTFE. Cyanate ester resin systems are being developed by a number of companies. Table 2 lists some of the major physical properties for various resin systems. They have been grouped into epoxy, polyimide, PTFE, and cyanate ester. The actual properties vary somewhat about these norms due to the differences in manufacturer formulations.

Table 3. Copper Foil Classes

Class	Description
1	Standard electrodeposited (STD, type E)
2	High-ductility electrodeposited (HD, type E)
3	High-temperature elongation electrodeposited (THE, type E)
4	Annealed electrodeposited (ANN, type E)
5	As-rolled wrought (AR, type W)
6	Light cold rolled-wrought (LCR, type W)
7	Annealed-wrought (ANN, type W)
8	As-roller-wrought-low-temperature annealable (ARLT, type W)

Metals in Laminates. The third major component of a PWB laminate is the metal used to create the interconnection circuitry. Copper is used almost exclusively. In thin-film multichip module applications, aluminum is sometimes used as the interconnect metal. Two types of copper foils are used in PWB applications; electrodeposited (E), the most prevalent, and wrought (W). The wrought foils are usually limited to special applications such as flexible printed circuits where high ductility is essential. The electrodeposited and wrought types are further subdivided into classes to reflect functional performance and testing properties. Table 3 lists the eight class descriptions.

Class 1, 2, 3, and 4 electrodeposited foils are used predominantly in laminates. Class 1 and 2 foils are more brittle and are not generally used in high-performance laminate applications where substantial thermal stress ranges are to be incurred. In class 1 foils, fracture without deformation will occur under relatively low stress levels. Class 3 and 4 foils are much more ductile at elevated temperatures and as such are used in the higher thermal stress environments. As mentioned, copper foil thicknesses are described in terms of area weight (oz/ft²). The various common foil are shown in Table 4. The side of copper foil, which is to be bonded to the laminate, may undergo a treatment to promote better adhesion. The copper foil treatment is an adhesion promoter selective for the resin being used. It is usually some form of black oxide treatment. Oxidation materials are generally known to provide optimized bond strength for most bonding systems. Failure to achieve an optimum bond of copper foil to results in poor bond strength of the etched copper circuits, a very important factor in PWB performance and reliability. SMT application requiring a controlled PWB CTE have led to the use of clad metals in PWB application. These metals used are either invar or molybdenum clad on their outer surface with copper. The thickness ration of invar or molybdenum to copper controls the CTE of the clad metal. The ratio of the thickness of the clad metal to the thickness of the laminate dielectric as well as their respective CTE's and elastic moduli determine the CTE of the overall PWB.

Laminate Types. Organic PWB laminates are by far the largest group of materials used for PWB applications in the electronic industry. Combining materials from the three major groups discussed—fabric, resin, and metal—leads to a wide variety of available laminates whose properties are tailored to meet specific PWB application requirements. There are strong industry standards for the laminates and the PWBs made using these laminates. The major groups that issue these standards are the National Electrical Manufacturers Association (NEMA), the Department of Defense (DOD) (for military specifications), and the Institute for Interconnecting and Packaging Electronic Circuits (IPC). IPC is an important major industry association whose documents include test standards, workmanship standards, PWB operations standards, and much more. The major NEMA standard grades for PWB laminates are listed in Table 5. The NEMA standard grades are used in a variety of commercial applications. FR-2, FR-3, CEM-1, CEM-3, FR-4, FR-5, are most widely

Table 4. Copper Foil Thickness Classifications

Designator	Thickness by Weight (oz/R ²)	Thickness by Weight (g/cm ²)	Thickness by Gauge (in.) Nominal	Thickness by Gauge (mm) Nominal
E	0.146 (1/8)	44.47	0.0002	0.005
O	0.263 (1/4)	80.18	0.0004	0.009
T	0.350 (3/8)	106.9	0.0005	0.012
H	0.500 (1/2)	153	0.0007	0.018
M	0.750 (3/4)	229	0.0010	0.025
1	1	305	0.0014	0.035
2	2	610	0.0028	0.071
3	3	915	0.0042	0.106
4	4	1221	0.0056	0.142
5	5	1526	0.0071	0.178
6	6	1831	0.0084	0.213
7	7	2136	0.0096	0.249
10	10	3052	0.0140	0.355
14	14	4272	0.0196	0.496

Table 5. Major Laminate Grades and Their Properties

NEMA Grade	Military Designation	Resin System	Base	Color	Operating Temp. (°C)	Description
XXXXC	None	Phenolic	Paper	Opaque brown	125	Phenolic pap
FR-2	None	Phenolic	Paper	Opaque brown	105	Phenolic pap
FR-3	FX	Epoxy	Paper	Opaque brown	105	Epoxy resin
CEM-1	None	Epoxy	Paper-glass	Opaque tan	130	Epoxy resin
CEM-3	None	Epoxy	Glass matt	Translucent	130	Epoxy resin
FR-6	None	Polyester	Glass matt	Opaque white	105	Polyester, re
G-10	GE	Epoxy	Glass	Translucent	130	Epoxy-glass
FR-4	GF	Epoxy	Glass	Translucent	130	Epoxy-glass
G-11	GP	Epoxy	Glass	Translucent	170	High-tempera
FR-5	GH	Epoxy	Glass	Translucent	170	High-tempera
GT	GT	PTFE	Glass	Opaque brown	220	Glass fabric
GX	GX	PTFE	Glass	Opaque brown	220	Glass fabric
		Polystyrene	Glass	Opaque white	220	Polystyrene
		Polyethylene	Glass	Opaque white	220	Polyethylene

used. The paper-based FR-2 laminates are used in low-cost consumer products such as toys, video games, and calculators. The FR-3 laminate, with its higher electrical and physical properties, is used in televisions, computers, and communication equipment. CEM-1 laminate has punching properties similar to FR-2 and FR-3, but with electrical properties approaching those of FR-4. It is used in industrial electronics, automobiles, and smoke detectors. CEM-3 is higher in cost than CEM-1 and is more suited for plated-through-hole (PTH) applications. FR-4 is the most widely used laminate material, due to its excellent physical, electrical, and processing properties. It is used in aerospace, computer, automotive, portable consumer communication, and industrial control applications. FR-5 is used in applications requiring higher heat resistance than attainable with FR-4. GT and GX are used in high-frequency applications.

Flexible PWB Materials. The materials and the anatomy of flexible printed wiring are different from those of the various rigid PWB constructions. Flexible printed wiring is etched or formed to the desired circuit pattern, and thus similar to rigid PWBs, except that it is flexible in form. The flexible circuit in both flexible and rigid-flex consists of three important materials: (1) base film, (2) conductor, and (3) adhesive. The metal foil is bonded and subsequently etched to the desired pattern on the adhesive-coated base film. A second adhesive-coated film is bonded on top of the formed circuit pattern. This top adhesive-coated film is usually the same material construction as the bottom, or base, adhesive-coated film. The top adhesive-coated film is known as the cover coat film.

BIBLIOGRAPHY

1. J. Aday T. Tessier J. Rasul A comparative analysis of high density PWB technologies, *Int. J. Microelectron. and Electron. Packaging*, **19** (4):404-411, 1996.
2. D. Bergman HDIS: Where standardization is headed, *CircuitTree*, **11** (3): 10, 12, 16, 18, 20, 1998.
3. T. Buck M. Motazedzi Microwire Interconnection Technology, PCK Technology Division, Kollmorgen Corp., July 1989.
4. C. F. Coombs, Jr. *Printed Circuits Handbook*, 4th ed., New York: McGraw-Hill, 1995.
5. W. S. Deforest *Photoresist Materials and Processes*, New York: McGraw-Hill, 1975.
6. C. A. Harper *Electronic Packaging and Interconnection Handbook*, 2nd ed., New York: McGraw-Hill, 1997.
7. H. Lee K. Neville *Handbook of Epoxy Resins*, New York: McGraw-Hill, 1982.
8. M. B. Miller *Dictionary of Electronic Packaging, Microelectronic, and Interconnection Terms*, Lutherville, MD: Technology Seminars, 1990.
9. J. Rasul W. Bratschun J. McGowen Microvia Bare Board Reliability Testing, *Proc. Tech. Conf., Inst. Interconnecting and Packaging Electron. Circuits (IPC) Printed Circuits Expo '97*, 1997.
10. D. P. Seraphim R. C. Lasky C. Y. Li *Principles of Electronic Packaging*, New York: McGraw-Hill, 1989.
11. R. L. Swiggett *Introduction to Printed Circuits*, New York: Rider, 1956.

JAD S. RASUL
Motorola Inc.