UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HEUNG-BAE LEE, GEA-OK CHO, and CHUN-DEOK SUH

Appeal 2008-3266
Application 09/949,076[1]
Technology Center 2600

Decided: October 29, 2008

Before ROBERT E. NAPPI, SCOTT R. BOALICK, and
JOHN A. JEFFERY, *Administrative Patent Judges*.

BOALICK, *Administrative Patent Judge*.

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[1] Application filed September 10, 2001. Application 09/949,076 claims the benefit under 35 U.S.C. § 119 of Korean application 2001-5073, filed February 2, 2001. The real party in interest is Samsung Electronics Co., Ltd.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1 and 10-13.[2] An oral hearing on this appeal was conducted on October 21, 2008. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

STATEMENT OF THE CASE

Appellants' invention relates to a data slicer in a Radio Frequency (RF) receiver that generates a pulse data signal by, among other things, deleting a Direct Current (DC) component from the received RF signal. (Spec. 1:5-8.)

Claim 1 is exemplary:

1. A data slicer comprising:

> a sample signal output portion for outputting a first sample signal by sequentially outputting samples of demodulated input signals that are sampled according to a predetermined sampling frequency, and outputting a second sample signal which is sampled at a predetermined time delayed from the first sample signal; and
>
> a data recovery portion for recovering the demodulated input signals into a DC offset component-deleted signal, by using the first and the second sample signals output from the sample signal output portion.

[2] Claims 2-9 have been indicated to be allowable if rewritten in independent form.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Goff	4,115,811	Sept. 19, 1978
Marko, et al.	5,402,448	Mar. 28, 1995
Büchler	6,169,716 B1	Jan. 2, 2001
Popplewell, et. al.	2002/0172301 A1	Nov. 21, 2002

Claims 1 and 10 stand rejected under 35 U.S.C. § 103(a) as being obvious over Popplewell and Büchler.

Claim 11 stands rejected under 35 U.S.C. § 103(a) as being obvious over Popplewell and Goff.

Claims 12 and 13 stand rejected under 35 U.S.C. § 103(a) as being obvious over Popplewell, Büchler, and Marko.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Briefs and the Answer for their respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments that Appellants did not make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).[3]

ISSUE

The issue is whether Appellants have shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 103(a). The issue turns on whether

[3] Except as will be noted in this opinion, Appellants have not presented any substantive arguments directed separately to the patentability of the dependent claims or related claims in each group. In the absence of a separate argument with respect to those claims, they stand or fall with the representative independent claim. *See* 37 C.F.R. § 41.37(c)(1)(vii).

the applied references teach or suggest outputting a second sample signal which is sampled at a predetermined time delay from the first sample signal and using the first and second sample signals to recover a DC offset component-deleted signal.

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. Popplewell describes a data slicer. (Paragraph [0001].) The data slicer includes "means to use knowledge of the value of an input signal received on at least one clock cycle preceding a current clock cycle to estimate where in the period of a read signal a present sample value relates to, and means to provide an output signal using extrapolation of the preceding values." (Paragraph [0008].)

2. Figure 1 of Popplewell shows "a digital phase-lock loop in which a data slicer in accordance with the present invention can be incorporated." (Paragraph [0015].) The digital phase lock loop includes a digital phase detector 5. (Paragraph [0019].)

3. Figure 3 of Popplewell "shows the phase detector [5] of the FIG. 1 phase-lock loop." (Paragraph [0017].) The phase detector 5 includes a data slicer 22 that examines digital value Y_n, which represents the amplitude of the read signal, on first digital line 10. (Paragraphs [0020] and [0034] through [0035].) The data slicer 22 then

determines the ideal sample value of Y_n and provides the ideal sample value on digital line 27 as X_n. (Paragraphs [0035], [0036].) In particular, "the data slicer **22** uses knowledge of the value of Y_n received on preceding clock cycles to estimate where in the period of the read signal **20** the present sample value relates to, and determine[s] X_n using extrapolation of preceding values of Y_n and examination of the current value of Y_n." (Paragraph [0036].) "This alternative provides a phase detector **5** which is less likely to determine an incorrect value of X_n in the face of a noisy read signal **20** than the conventional data slicer arrangement." (*Id.*) Digital line 27 carries the value of X_n provided by the data slicer 22 to a subtracter device 28 and to a delay register 29. (Paragraph [0042].)

4. Figure 4 of Popplewell "shows a data slicer [22] in accordance with the present invention, forming part of the phase detector [5] of FIG. 3." (Paragraph [0018].) The data slicer 22 includes "a threshold slicer **60**, first and second digital switches **61, 62**, a state logic device **63** and a state to slice converter device **64**." (Paragraph [0037].) "The digital line **10** is connected to the input of the threshold slicer **60** which provides, on an output line **65**, a sliced value, which is thereby provided to a first input of the switch **62**." (Paragraph [0038].) In providing the sliced value on digital line 65, the threshold slicer 60 operates in the same way as a conventional data slicer. (*Id.*)

5. Continuing to refer to Figure 4 of Popplewell, "[t]he threshold slicer **60** further includes logic arranged to provide a digital signal on a

digital line **66** which identifies the starting state of a state machine." (Paragraph [0038].) "The starting state is determined by observing the sliced valves [sic, values] for two successive slicer levels which correspond to a valid succession of slicer levels." (*Id.*) The value provided on line 66 "identifies the starting state of the state machine based on the first two initial valid threshold states." (*Id.*) "The state logic device **63** receives the starting state, determined by logic in the threshold slicer **60**, from the digital line **66**." (Paragraph [0040].) "The state logic device **63** initiates itself using the starting state so received and thereafter cycles sequentially through the states with the frequency of the sampling clock." (*Id.*) "[T]he output of the data slicer **22** is determined by the state logic device **63** and the sampling clock and is thus not susceptible to slicing errors occurring in the threshold slicer **60**." (Paragraph [0041].)

6. Büchler describes a data slicer that compensates for a DC voltage offset. (Col. 2, ll. 52-67.)

PRINCIPLES OF LAW

All timely filed evidence and properly presented arguments are considered by the Board in resolving an obviousness issue on appeal. *See In re Piasecki*, 745 F.2d 1468, 1472 (Fed. Cir. 1984).

In the examination of a patent application, the Examiner bears the initial burden of showing a prima facie case of unpatentability. *Id.* at 1472. When that burden is met, the burden then shifts to the Applicant to rebut. *Id.*; *see also In re Harris*, 409 F.3d 1339, 1343-44 (Fed. Cir. 2005) (finding

rebuttal evidence unpersuasive). If the Applicant produces rebuttal evidence of adequate weight, the prima facie case of unpatentability is dissipated. *In re Piasecki*, 745 F.2d at 1472. Thereafter, patentability is determined in view of the entire record. *Id.* However, on appeal to the Board it is the Appellant's burden to establish that the Examiner did not sustain the necessary burden and to show that the Examiner erred. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006).

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1734 (2007). "[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d at 988.

During examination of a patent application, a claim is given its broadest reasonable construction consistent with the specification. *In re Prater*, 415 F.2d 1393, 1404-05 (CCPA 1969). "[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted). The "ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1313.

ANALYSIS

Appellants contend that the Examiner erred in rejecting claims 1 and 10-13. Reviewing the record before us, we agree. In particular, we find that the Appellants have shown that the Examiner failed to make a prima facie showing of obviousness with respect to claims 1 and 10-13.

Regarding claim 1, Appellants argue that Popplewell and Büchler do not teach or suggest a second sample signal, as claimed. (App. Br. 12-14; Reply Br. 4-8.) In particular, Appellants argue that Popplewell and Büchler do not teach or suggest a second sample signal which is sampled at a predetermined time delay from a first sample signal and is used for recovering a DC offset component-deleted signal. (App. Br. 12; Reply Br. 6-7.) We agree.

The Examiner found that Popplewell disclosed a data slicer 22 that outputs a second sample signal 66 which is sampled at a predetermined time delay from a first sample signal 65. (Ans. 4.) The Examiner also found that, although Popplewell "is silent regarding recovering the demodulated input signals into a DC offset component-deleted signal, by using the first and second sample signals" (Ans. 4), Büchler discloses this limitation. (Ans. 4-5.) The Examiner found that "[i]t would have been obvious to one skilled in the art at the time the invention was made to use the data recovery circuit taught by Büchler in the data slicer of Popplewell so as to optimize and ensure [the] output signal is free from DC voltage offset." (Ans. 5.)

Initially, we agree with the Examiner that line 66 of Popplewell's data slicer 22 broadly may be interpreted as a second signal that is sampled at a predetermined time delay from first signal 65. Popplewell teaches that knowledge of an input signal value on at least one clock cycle preceding a

current clock cycle is used to estimate where in the period of a read signal a present sample value relates to. (FF 1, 3.) In particular, Popplewell teaches that a digital signal that identifies the starting state of a state machine is provided on line 66 by observing the sliced valves for two successive slicer levels. (FF 5.) Thus, under the broadest reasonable interpretation of the claim, Popplewell teaches a second signal sampled at a predetermined time delay from a first signal.[4]

However, the Examiner has not shown, nor do we find, any teaching or suggestion to use the second signal (on line 66) of Popplewell in order to recover a DC offset component-deleted signal. Indeed, we agree with Appellants that the signal on line 66, as taught by Popplewell, could not be used to produce a DC offset component-deleted signal. (App. Br. 12.) Line 66 provides a signal that identifies the starting state of state machine, and is used to initiate state logic device 63. (FF 5.) After state logic device 63 initiates itself using that starting state, it "thereafter cycles sequentially through the states with the frequency of the sampling clock." (FF 5.) In other words, the signal on line 66 is used only to initialize state logic device 63. Büchler does not remedy the deficiencies of Popplewell. Although Büchler describes removing a DC offset (FF 6), it does not teach how a signal such as the state machine initialization signal on line 66 of Popplewell could be used in the removal of the DC offset. Thus, the

[4] Although the Examiner also pointed to the delay register 29 shown in Figure 3 to teach a delayed second sample signal (Ans. 8-9), we note that delay register 29 is not part of data slicer 22. Instead, both are separate components of the phase detector 5. (FF 3.) Indeed, delay register 29 receives the output signal X_n from data slicer 22. (FF 3.) Thus, we do not see how delay register 29 is relevant to show a second sample signal in data slicer 22.

Examiner has not shown, and we do not find, any convincing evidence of a teaching or suggestion in the applied references of a second signal that is used to recover a DC offset component-deleted signal, as claimed.

Accordingly, we conclude that Appellants have shown that the Examiner erred in rejecting claim 1 under 35 U.S.C. § 103(a). Independent claims 10, 11, and 12 recite limitations similar to those discussed with respect to claim 1. Because Goff and Marko, which were variously combined with Popplewell and/or Büchler to reject claims 10, 11, and 12, do not remedy the deficiencies of Popplewell and/or Büchler discussed with respect to claim 1, we conclude that Appellants have shown that the Examiner erred in rejecting independent claims 10, 11, and 12, and dependent claim 13 which depends from claim 12, for the reasons discussed with respect to claim 1.

CONCLUSION OF LAW

We conclude that Appellants have shown that the Examiner erred in rejecting claims 1 and 10-13 for obviousness under 35 U.S.C. § 103(a).

DECISION

The rejection of claims 1 and 10-13 for obviousness under 35 U.S.C. § 103(a) is reversed.

REVERSED

MAT

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