

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DIRK LEIPOLD

Appeal 2008-3924
Application 09/798,106
Technology Center 2800

Decided: December 8, 2008

Before THOMAS A. WALTZ, JEFFREY T. SMITH, and
KAREN M. HASTINGS, *Administrative Patent Judges*.

HASTINGS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134 from the Examiner's decision rejecting claims 1, 3-6 and 8-12. We have jurisdiction under 35 U.S.C. § 6.

We AFFIRM.

Appellant claims a method of forming a buried layer in a complementary metal oxide semiconductor (i.e., CMOS) structure.

Representative claim 1 reads as follows (italics provided):

1. A method of forming a buried layer in a CMOS structure, comprising:
 - a) *forming a first mask to define first conductivity-type wells* in a semiconductor layer.
 - b) implanting first conductivity-type dopants into said semiconductor layer using said first mask to form a first well and a first buried region;
 - c) *forming a second mask to define said second conductivity-type wells* in said semiconductor layer; and
 - d) implanting first and second conductivity-type dopants into said semiconductor layer using said second mask to form a second well from the second conductivity-type dopants and a second buried region from the first conductivity-type dopants with said second buried region at about the same depth as said first buried region, *whereby a first conductivity-type buried layer under said wells* is formed from said first and second buried region.

The prior art set forth below is applied by the Examiner in the § 103 rejections before us as evidence of unpatentability:

Sung	5,573,963	Nov. 12, 1996
Sim	6,097,078	Aug. 1, 2000

Claims 1, 3-6, and 8-12 are rejected under the second paragraph of 35 U.S.C. § 112 for failing to particularly point out and distinctly claim the subject matter which Appellant regards as the invention.

Claims 1, 5-6, 8, 11, and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sim.

Claims 3, 4, 9, and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sim in view of Sung.

Within the first and second grounds of rejection, Appellant has not separately argued any claim with any reasonable degree of specificity. (App. Br. 4-5). Thus, in accordance with 37 C.F.R. § 41.37(c)(1)(vii), we select claim 1 as representative for each of these grounds of rejection. With respect to the third ground of rejection, Appellant relies only on the arguments presented for the second ground of rejection.

THE § 112, SECOND PARAGRAPH, REJECTION

ISSUE

Has the Examiner erred in holding that the claims are indefinite within the meaning of 35 U.S.C. § 112, second paragraph? This issue turns on whether the language *in italics* of claim 1 above, when read in light of the Specification, fails to particularly point out and distinctly claim what Appellant regards as the invention.

PRINCIPLE OF LAW

The test for definiteness under 35 U.S.C. § 112, second paragraph, is whether “those skilled in the art would understand what is claimed when the claim is read in light of the specification.” *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576 (Fed. Cir. 1986) (citations omitted); *see also In re Warmerdam*, 33 F.3d 1354, 1361 (Fed. Cir. 1994) (“The legal standard for definiteness is whether a claim reasonably apprises those of skill in the art of its scope.”), and *In re Moore*, 439 F.2d 1232, 1235 (CCPA 1971) (the definiteness of the language employed in a claim must be

analyzed not in a vacuum, but in light of the teachings of the particular application).

FINDING OF FACTS
AND ANALYSIS

The Examiner contends that since Appellant's Figs. 3 and 4 depict only one opening for a first well and one opening for a second well, the limitations of claim 1 which recite "forming a first mask to define first ... wells" and "forming a second mask to define second ... wells" are unclear (Ans. 3-4).

As the Specification points out, Appellant's drawings show only a single p-well and a single n-well in a semiconductor for clarity (see, e.g., Spec. 3, line 12). As Appellant notes, a single example of each of a plurality of same type wells in a semiconductor device may be illustrated to avoid replication (Br. 5).

The Specification is clear that the claimed first and second masks will include multiple openings in order to define "first conductivity type *wells*" and "second conductivity type *wells*" as claimed in claim 1 (Spec. 5, description of steps (2) and (3); emphasis provided). Thus, the disputed language of claim 1 reasonably apprises those skilled in the art of the scope of the invention.

The Examiner also contends that it is not understood what "wells" are being referred to in the limitation "a first buried layer under said wells" in the final clause of claim 1. One of ordinary skill in the art would understand that "under said wells" at the end of claim 1 means under all the wells previously recited in the claim (Br. 5).

CONCLUSION OF LAW

For the above stated reasons, the Examiner erred in holding that the claims are indefinite within the meaning of 35 U.S.C. § 112, second paragraph. Accordingly, we do not sustain the § 112, second paragraph, rejection of claims 1, 3-6 and 8-12.

THE § 103 REJECTIONS

ISSUE

The Examiner relies upon Figs. 6-11 and the related description thereof to find that Sim describes a method for forming a semiconductor with a triple well structure that includes all the steps set out in the body of claim 1 (Ans. 4). The Examiner concludes that the claimed invention would have been *prima facie* obvious in view of these teachings of Sim (Ans. 5).

Appellant only contends that Sim does not expressly teach that a buried n-layer is under the p-well 210 of Fig. 2 of Sim (Br. 5).

The issue before us is did Appellant identify reversible error in the Examiner's § 103 rejection of claim 1? The issue turns on whether it would have been *prima facie* obvious to a person of ordinary skill in the art to have used the technique of forming an n-layer under a p-type well as shown in Sim's semiconductor device for forming a buried layer "in a CMOS structure".

FINDINGS OF FACT

Sim describes, as prior art, a complementary metal oxide semiconductor (CMOS) dynamic random access memory (DRAM) device

(col. 1, ll. 10-19). Sim describes an improved “triple well structure” has been suggested for CMOS DRAM devices (col. 1, ll. 19-25).

Fig. 1 of Sim depicts the admitted prior art triple well structure.

Sim then describes various embodiments of an improved method of manufacturing a triple well structure (col. 2, ll. 1-7). Fig. 2-5 of Sim are one embodiment, Fig. 6-9 illustrate a second embodiment, and Fig. 10-11 illustrate a third embodiment (col. 2, ll. 59-67). This third embodiment is a combination of the first and second embodiments (col. 5, ll. 55-58). Thus, there are common features to the second and third embodiments as well.

The Examiner relies upon Figs. 6-11 to find that Sim describes a method for forming a semiconductor with a triple well structure that includes all the steps set out in the body of claim 1 (Ans. 4).

One having ordinary skill in the art would have understood that Sim describes a general technique for forming a buried layer of a first conductivity-type underneath a well of a second conductivity-type in a semiconductor device.

PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) (“On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.”) (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

A claimed invention is not patentable if the subject matter of the claimed invention would have been obvious to a person having ordinary skill in the art. 35 U.S.C. § 103(a); *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727 (2007); *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1 (1966).

Under 35 U.S.C. § 103, the factual inquiry into obviousness requires a determination of: (1) the scope and content of the prior art; (2) the differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966).

“The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1739 (2007). The question to be asked is “whether the improvement is more than the predictable use of prior art elements according to their established functions.” *KSR*, 127 S. Ct. at 1740.

It is a basic principle that the question under 35 U.S.C. § 103 is not merely what the references expressly teach but what they would have suggested to one of ordinary skill in the art at the time the invention was made. *See Merck & Co. v. Biocraft Labs., Inc.*, 874 F.2d 804, 807 (Fed. Cir. 1989).

Nor is it necessary that suggestion or motivation be found within the four corners of the references themselves. “The obviousness analysis cannot be confined by the formalistic conception of the words teaching, suggestion and motivation, or by overemphasis on the importance of . . . the explicit content of issued patents.” *KSR*, 127 S. Ct. at 1741. The Supreme Court also noted in *KSR* that an obviousness analysis “need not seek out precise

teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.” *Id.*

In *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007), the Federal Circuit found no error in the District Court's determination that a combination of elements was proper in part because Leapfrog had presented no evidence that the inclusion of a reader in the combined device was “uniquely challenging or difficult for one of ordinary skill in the art” or “represented an unobvious step over the prior art.” *Id.* (citing *KSR*, 127 S. Ct. at 1740-41).

ANALYSIS

Sim describes forming a buried layer in a semiconductor structure using the steps recited in the body of claim 1. Sim describes forming buried regions of the same conductivity type under n- and p-type wells in a semiconductor device. The Examiner acknowledges that Sim does not explicitly describe that these steps are for forming a buried layer “in a CMOS structure” as recited in the preamble of claim 1 (Ans. 5).

In essence, since the claimed steps of claim 1 are known for use in making a buried layer in the semiconductor device (i.e., a CMOS DRAM device) of Sim, we agree with the Examiner’s implicit conclusion that a person of ordinary skill in the art would have reasonably expected that known steps for forming a buried layer in the semiconductor device would have been suitable for forming a buried layer “in a CMOS structure” which is an admittedly known prior art structure.

Thus, using the steps taught in Sim for forming a buried layer “in a CMOS structure” appears to be no more than the predictable use of these

prior art method steps according to their established functions of forming a buried layer underneath conductivity type wells in a semiconductor structure. *KSR*, 127 S. Ct. at 1740.

Appellant only contends that Sim does **not** describe that a buried n-layer is under the p-well 210 of Fig. 2 of Sim; that is, “Sim Fig. 2 . . . shows . . . no implant of n-type dopants for a buried layer under the p-well.” (Br. 5). Although this is true, this does not answer the question of whether it would have been *prima facie* obvious to a person of ordinary skill in the art to have used the technique of forming an n-layer under a p-type well as shown in Sim’s semiconductor device for forming a buried layer “in a CMOS structure”.

Appellant has not contended that it would take more than ordinary creativity to use these known steps of Sim to form a buried layer “in a CMOS structure”. See, e.g., *Leapfrog*, 485 F.3d at 1162. For example only, Appellant does not present *any* reasoning or evidence that a CMOS structure with one conductivity type buried layer underneath both a p-well and n-well of the “CMOS structure” is not known in the prior art.

We therefore agree with the Examiner that the Appellant has not “rebutted the validity of the obviousness statement” (Ans. 9).

CONCLUSIONS OF LAW

Appellant has not shown that the Examiner erred in determining that it would have been *prima facie* obvious to a person of ordinary skill in the art to have used the technique of forming an n-layer under a p-type well as shown in Sim’s semiconductor device for forming a buried layer “in a

Appeal 2008-3924
Application 09/798,106

CMOS structure.” It follows that we sustain the § 103 rejection of claims 1, 5, 6, 8, 11, and 12 as unpatentable over Sim.

No additional argument has been made by Appellant regarding the § 103 rejection of claims 3, 4, 9, and 10 based on Sim and Sung. Therefore, we also sustain the § 103 rejection of claims 3, 4, 9, and 10 advanced by the Examiner in this appeal.

ORDER

The decision of the Examiner is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

ls

TEXAS INSTRUMENTS INCORPORATED
P.O. BOX 655474, M/S 3999
DALLAS, TX 75265