

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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*Ex parte* CRAIG T. SWIFT, GOWRISHANKAR L. CHINDALORE,  
and LAUREEN H. PARKER

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Appeal 2008-4053  
Application 10/961,295<sup>1</sup>  
Technology Center 2800

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Decided: September 15, 2008

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Before MAHSHID D. SAADAT, SCOTT R. BOALICK,  
and JOHN A. JEFFERY, *Administrative Patent Judges*.

BOALICK, *Administrative Patent Judge*.

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<sup>1</sup> Application filed October 8, 2004. The real party in interest is Freescale Semiconductor, Inc.

## DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1-3, 5, 7, 9, 11, and 25-31. Claims 12-24 have been withdrawn from consideration (Br. 2). We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

## STATEMENT OF THE CASE

Appellants' invention relates to a virtual ground memory array with enhanced separation between the source/drain and word line (gate) of the memory transistors. (Spec. 1:13-15.)

Claim 1 is exemplary:

1. A semiconductor device comprising:
  - a semiconductor substrate;
  - a doped region in the semiconductor substrate;
  - a charge storage layer over the semiconductor substrate having a top surface that is substantially planar;
  - a first gate conductor over a first portion of the charge storage layer;
  - a second gate conductor over a second portion of the charge storage layer;
  - an insulating region over the doped region and between the first gate conductor and the second gate conductor and having a bottom surface that is substantially coplanar with the top surface of the charge storage layer; and

a word line over the insulating region and contacting the first gate conductor and the second gate conductor.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Fujiwara

US 6,191,445 B1

Feb. 20, 2001

Claims 1-3, 5, 7, 9, 11, and 25-31 stand rejected under 35 U.S.C. § 103(a) as being obvious over Fujiwara.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Brief and the Answer for their respective details.<sup>2</sup>

#### ISSUE

The issue is whether Appellants have shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 103(a). The issue turns on whether Fujiwara teaches or suggests a semiconductor device having an insulating region over a doped region and between (1) a first gate conductor over a first portion of a charge storage layer and (2) a second gate conductor over a second portion of the charge storage layer, and also having a bottom surface that is substantially coplanar with the top surface of the charge storage layer.

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<sup>2</sup> Except as will be noted in this opinion, Appellants have not presented any substantive arguments directed separately to the patentability of the dependent claims. In the absence of a separate argument with respect to those claims, they stand or fall with the representative independent claim. *See* 37 C.F.R. § 41.37(c)(1)(vii).

## PRINCIPLES OF LAW

All timely filed evidence and properly presented arguments are considered by the Board in resolving an obviousness issue on appeal. *See In re Piasecki*, 745 F.2d 1468, 1472 (Fed. Cir. 1984).

In the examination of a patent application, the Examiner bears the initial burden of showing a prima facie case of unpatentability. *Id.* at 1472. When that burden is met, the burden then shifts to the Applicant to rebut. *Id.*; *see also In re Harris*, 409 F.3d 1339, 1343-44 (Fed. Cir. 2005) (finding rebuttal evidence unpersuasive). If the Applicant produces rebuttal evidence of adequate weight, the prima facie case of unpatentability is dissipated. *In re Piasecki*, 745 F.2d at 1472. Thereafter, patentability is determined in view of the entire record. *Id.* However, on appeal to the Board it is the Appellant's burden to establish that the Examiner did not sustain the necessary burden and to show that the Examiner erred. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006).

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1734 (2007).

"[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d at 988. "To facilitate review, this analysis should be made explicit." *KSR*, 127 S. Ct. at 1741.

During examination of a patent application, a claim is given its broadest reasonable construction consistent with the specification. *In re Prater*, 415 F.2d 1393, 1404-05 (CCPA 1969). "[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted). The "ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1313.

#### ANALYSIS

Appellants contend that the Examiner erred in rejecting claims 1-3, 5, 7, 9, 11, and 25-31 as being obvious over Fujiwara. Reviewing the record before us, we agree.

Regarding claim 1, Appellants argue that the Examiner has not shown that Fujiwara teaches or discloses an insulating region over a doped region and between (1) a first gate conductor over a first portion of a charge storage layer and (2) a second gate conductor over a second portion of the charge storage layer, as claimed. (Br. 5-6.) Appellants also argue that the Examiner has not shown that Fujiwara teaches or suggests an insulating region having a bottom surface that is substantially coplanar with the top surface of the charge storage layer, as claimed. (Br. 6.) We agree.

The Examiner found that Fujiwara discloses a first gate conductor 8 over a first portion of a charge storage layer 12. (Ans. 3-4; Fujiwara, Fig. 1.) We agree with this finding. The Examiner then found that Figures 1 and 15 of Fujiwara shows a second gate conductor over a second portion of the

charge storage layer as well as an insulating region 71 over the doped region and between the first and second gate conductors having a bottom surface that is substantially coplanar with the top surface of the charge storage layer. (Ans. 3-4, 8-10; Fujiwara, Figs. 1, 15.) To further explain this finding, the Examiner's Answer provided a composite drawing showing Figures 1 and 15 of Fujiwara in relation to Figure 3 of the instant application. (Ans. 9.) In that drawing, the Examiner equated bit lines  $BL_{n-1}$ ,  $BL_n$ , and  $BL_{n+1}$  in Figure 15 of Fujiwara, which are pointed to by arrows A, C, and E, with first, second, and third gate conductors. (Ans. 8-9.) The Examiner also equated isolation regions 71, which are pointed to by arrows B and D, with the claimed insulating region. (Ans. 8-9.) We do not agree with these findings.

Although the Examiner equates bit lines  $BL_{n-1}$ ,  $BL_n$ , and  $BL_{n+1}$  to the claimed gate conductors (Ans. 8-9), Fujiwara teaches that these bit lines are connected to drain regions of the memory transistors -- not to gate conductors. (Fujiwara, col. 23, ll. 18-23.) In addition, the charge storage layer 12 of Figure 1 is shown as being coextensive with the first gate conductor 8, and the Examiner has not shown that Fujiwara teaches or suggests that the charge storage layer 12 extends beyond the first gate conductor 8. In other words, the Examiner has not pointed to, nor do we find, a teaching or suggestion in Fujiwara that a second gate conductor is located over a *second portion* of charge storage layer 12. Furthermore, while Figure 15 shows isolation regions 71 between bit lines  $BL_{n-1}$ ,  $BL_n$ , and  $BL_{n+1}$ , Fujiwara does not disclose or describe how or where these isolation regions 71 are formed. For example, there is no figure in Fujiwara showing a profile view of isolation region 71. Therefore, we do not find support for the Examiner's assertion (Ans. 4) that isolation regions 71 have a bottom

surface that is substantially coplanar with the top surface of the charge storage layer 12. The Examiner also appears to have equated insulating region 14 in Figure 1 of Fujiwara with the claimed insulating region. (Ans. 10.) However, the insulating region 14 is shown as being coextensive with the first gate conductor 8. (Fujiwara, Fig. 1.) The Examiner has not shown that Fujiwara teaches or suggests that the insulating region 14 of Figure 1 extends beyond the first gate conductor 8. In other words, while insulating region 14 has a bottom surface that is substantially coplanar to the charge storage layer 12, the Examiner has not pointed to, nor do we find, a teaching or suggestion in Fujiwara that insulating region 14 is located *between* first and second gate conductors, as claimed.

Thus, we agree with Appellants that Fujiwara does not teach or suggest a semiconductor device having an insulating region over a doped region and between (1) a first gate conductor over a first portion of a charge storage layer and (2) a second gate conductor over a second portion of the charge storage layer, and also having a bottom surface that is substantially coplanar with the top surface of the charge storage layer, as claimed. In addition, there is no evidence before us to show that this feature is a predictable variation of the prior art. Nor is there evidence before us to show that this feature would be common sense or a creative step that a person of ordinary skill in the art would employ.

Accordingly, we conclude that Appellants have shown that the Examiner erred in rejecting independent claim 1, and in rejecting claims 2, 3, 5, 7, 9, and 11 which depend from claim 1.

Independent claim 25 recites limitations similar to the limitations of claim 1 which we have found to be missing from Fujiwara. Therefore, we

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conclude that Appellants have shown that the Examiner erred in rejecting independent claim 25, and in rejecting claims 26-31 which ultimately depend from claim 25.

#### CONCLUSION OF LAW

We conclude that Appellants have shown that the Examiner erred in rejecting claims 1-3, 5, 7, 9, 11, and 25-31 for obviousness under 35 U.S.C. § 103.

#### DECISION

The rejection of claims 1-3, 5, 7, 9, 11, and 25-31 for obviousness under 35 U.S.C. § 103 is reversed.

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REVERSED

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