

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL A. VYVODA

Appeal 2008-4183
Application 10/440,882
Technology Center 2800

Decided: September 22, 2008

Before KENNETH W. HAIRSTON, MAHSHID D. SAADAT,
and SCOTT R. BOALICK, *Administrative Patent Judges*.

HAIRSTON, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. §§ 6(b) and 134 from the final rejection of claims 46 to 49.

The disclosed invention relates to a memory array that comprises a plurality of Schottky diodes or incipient Schottky diodes. In Figure 8D, the first Schottky diode or incipient Schottky diode is formed by the two layers that sandwich antifuse layer 204, and the second Schottky diode or incipient

Schottky diode is formed by the two layers that sandwich antifuse layer 216. The memory array includes a vertical interconnect formed by titanium nitride film 222 and doped polysilicon layer 223, and having a sidewall with a stair-step profile (Spec. 1, 4, 7, and 16 to 18).

Claim 46 is representative of the claimed invention, and it reads as follows:

46. A memory array comprising:
a plurality of Schottky diodes or incipient Schottky diodes; and
a vertical interconnect having a sidewall with a stair-step profile.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Ovshinsky	US 4,646,266	Feb. 24, 1987
Fricke	US 6,661,691 B2	Dec. 9, 2003 (filed Apr. 2, 2002)

The Examiner rejected claims 46 to 49 under 35 U.S.C. § 103(a) based upon the teachings of Ovshinsky and Fricke.

In the obviousness rejection of claims 46 to 49, the Examiner indicates that Ovshinsky describes a plurality of Schottky diodes or incipient Schottky diodes with a stair-step sidewall profile (Figs. 18 and 19) but lacks a vertical interconnect with a stair-step sidewall profile (Ans. 3). Fricke “shows (fig. 3) an interconnect structure (40) having a stair-step configuration to connect one or more memory cells in a first plane with one or more memory cells in another plane” (Ans. 3 and 4). According to the Examiner (Ans. 4), it would have been obvious to the skilled artisan “to modify the connecting pads on the stair-step profile of Ovshinsky by forming a metal conductor having a stair-step configuration as taught by

Fricke to connect one or more memory cells in a first plane with one or more memory cells in another plane.” Appellant contends that the introduction of a stair-step interconnection structure as taught by Fricke into Ovshinsky would electrically connect together all of the pads 190a in each of the input latches 140 and 144 and the output latch 142, and would be counter to the connection of each individual pad 190a to a separate pad 220 around the periphery of the mounting substrate 210 (App. Br. 6 and 7; Reply Br. 2 and 3).

Ovshinsky describes an integrated circuit with programmable logic array (PLA) devices 120, 122, and 124 arranged in a multi-level stair-step structure 110 (Fig. 18; col. 18, ll. 13 to 17). “The multi-layered structure 110 is terraced at its edge so that the input and output lines of each of the PLA layers 120 and 122 can be contacted by a respective down-bonded chip 140, 142, 144 or 146” (col. 18, ll. 57 to 61). Each of the chips 140, 142, 144, and 146 is connected to a contact pad 220 around the periphery of mounting substrate 210 via a bonding wire 222 and a contact pad 190a (Figs. 18 and 25; col. 24, ll. 8 to 29). In an alternative embodiment of an integrated circuit, Ovshinsky describes a plurality of Schottky diodes 12 and 14 that are not arranged in a stair-step profile (Fig. 19; col. 19, l. 56 to col. 21, l. 12). Fricke, like Ovshinsky, describes integrated circuits with PLA devices. The PLA devices in Fricke are designed to be connected together via stair-step interconnection 300 (Fig. 3; col. 4, ll. 31 to 38).

We agree with Appellant’s argument that each PLA device in Ovshinsky is designed for individual connection to the periphery of the mounting substrate, whereas the PLA devices in Fricke are designed to be

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connected together via a stair-step interconnection. We also agree with Appellant's argument that "[i]f pads 140, 142, 144, and 146 [in Ovshinsky] are connected to each other, the function of the device will be changed, and the device most likely rendered inoperable" and "unsatisfactory for its intended purpose" (App. Br. 7).

In summary, the obviousness rejection of claims 46 to 49 is reversed because the Examiner's articulated reasons for combining the teachings of Ovshinsky with those of Fricke do not support a legal conclusion of obviousness. *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727, 1741 (2007).

The decision of the Examiner is reversed.

REVERSED

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ESCHWEILER & ASSOCIATES, L.L.C.
NATIONAL CITY BANK BUILDING
629 EUCLID AVENUE, SUITE 1000
CLEVELAND, OH 44114