UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GEOFF BARRETT,
SIMON CHRISTOPHER DEQUIN CLEMOW, and
ANDREW JON DAWSON

Appeal 2008-4250
Application 10/284,294[1]
Technology Center 2100

Decided: December 12, 2008

Before JOSEPH L. DIXON, JEAN R. HOMERE, and
ST. JOHN COURTENAY III, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION ON APPEAL

I. STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1 through 36. We have jurisdiction under 35 U.S.C. § 6(b). We reverse.

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[1] Filed on October 31, 2002. The real party in interest is Broadcom Corp.

The Invention

Appellants invented a method and apparatus for progressively developing a logic model design for an integrated circuit. (Spec. 1.) As depicted in Figure 1, a logic designer compiles and optionally simulates a source file (110) to create a logic model (120), which is subsequently realized to produce a logic circuit (130). (Spec. 4.) Particularly, the invention aims at realizing and verifying the logic model design in a piecemeal fashion. (Spec. 2.) As shown in Figures 8 and 9, in the realization phase, the logic model (120) is fed to a logic development device (930) that divides it into two or more logic model portions, wherein each portion is separately realized. (Spec. 9-10.) Each realized logic portion is then fed to the wrapping device (950) to estimate or measure the resulting signals produced therefrom. (*Id*.) In the verification phase, each wrapped realized logic portion along with a corresponding logic model portion are fed to a verification device (960), and then fed to a comparing device (970) to verify that the logic portion is functioning correctly. If the comparing device indicates that the various outputs of the logic model portion and the realized logic portion are identical or sufficiently similar, then the wrapper is deemed to be correct. (*Id*.)

Illustrative Claim

Independent claim 1 further illustrates the invention. It reads as follows:

1. A method for realizing a logic model design, comprising:

dividing a logic model design into two or more logic model portions;

performing a realization step on a first logic model portion to produce a first realized logic portion;

applying a first wrapper to the first realized logic portion;

verifying the functionality of the first wrapped realized logic portion; and

verifying the functionality of the first wrapper if the first wrapped realized logic portion is verified to be functioning correctly.

Prior Art Relied Upon

The Examiner relies on the following prior art as evidence of unpatentability:

Okazaki	5,699,283	Dec. 16, 1997
Abts	6,856,950 B1	Feb. 15, 2005

Rejection on Appeal

The Examiner rejects the claims on appeal as follows:

Claims 1 through 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Okazaki and Abts.

Appellants' Contentions

Appellants argue that the combination of Okazaki and Abts does not render claims 1 through 36 unpatentable. (App. Br. 12-15, Reply Br. 2-5.) Particularly, Appellants argue that Okazaki is limited to verifying a whole logic design with logical changes by comparing it to the whole logic design prior to the logical changes. (App. Br. 13, Reply Br. 2.) However,

Appellants argue that neither Okazaki nor Abts teaches or suggests a piecemeal verification of the logic design by separately verifying the divided portions thereof, and by verifying in isolation the functionality of a wrapper even when a realized logic portion to which the wrapper is applied is verified to be functioning correctly. (*Id*.)

Examiner's Findings

The Examiner avers that Appellants' arguments are not commensurate in scope with the claims. Further, the Examiner finds that Okazaki's dividing unit, judging unit and compiling unit fairly teaches or suggests verifying the functionality of a wrapper if a corresponding wrapped realized logic is functioning correctly, as recited in independent claim 1. (Ans. 9-10.) Therefore, the Examiner concludes that the combination of Okazaki and Abts renders claim 1 unpatentable. (*Id*.)

II. ISSUE

The pivotal issue before us is whether Appellants have shown that the Examiner erred in concluding that the combination of Okazaki and Abts teaches upon verifying that a first wrapped realized logic portion of a logic model design is functioning correctly, verifying the functionality of the wrapper associated therewith, as recited in independent claim 1. We answer this inquiry in the affirmative.

III. FINDINGS OF FACT

The following findings of fact (FF) are supported by a preponderance of the evidence.

Okazaki

1. Okazaki discloses a logic emulation system for implementing changes in logical circuit. Particularly, Okazaki discloses a dividing unit for dividing design data on the logical circuit into LSI mapping data representing a plurality of small-scale circuits connected by PGA connections data. The LSI data and PGA connection data are mapped into programmable chips to thereby generate an equivalent circuit of the logical circuit. (Col. 2, ll. 44-50.)

2. The logic emulation system also includes a judging unit for comparing the design data including logical changes with the design data excluding the logical changes (i.e. LSI mapping-PGA connection data). Then the judging unit determines whether it is feasible to implement the logically changed logic circuit by adding small-scale circuits and by changing the PGA connection data. (Col. 2, ll. 55-59.)

3. If the judging means determines that the implementation of the logical changes in the logic circuit is feasible, the dividing unit generates the LSI mapping data that are mapped into programmable chips to thereby generate an equivalent circuit of the logically changed circuit. (Col. 2, ll. 60-65.)

IV. PRINCIPLES OF LAW

Claim Construction

"[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d at 1312 (internal citations omitted). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id*. at 1313.

"[T]he PTO gives claims their 'broadest reasonable interpretation.'" *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). "Moreover, limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989)). Our reviewing court has repeatedly warned against confining the claims to specific embodiments described in the specification. *Phillips v. AWH Corp.*, 415 F.3d at 1323.

Obviousness

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary

indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

> Section 103 forbids issuance of a patent when "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

KSR Int'l Co. v. Teleflex Inc., 127 S. Ct. 1727, 1734 (2007).

The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) wherein evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). *See also KSR*, 127 S. Ct. at 1734 ("While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.")

"The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Leapfrog Enter., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1161 (Fed. Cir. 2007) (quoting *KSR*, 127 S. Ct. at 1739). "One of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims." *KSR*, 127 S. Ct. at 1742.

The reasoning given as support for the conclusion of obviousness can be based on interrelated teachings of multiple patents, the effects of demands

known to the design community or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art. *KSR*, 127 S. Ct. at 1740-41. *See also Dystar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006).

V. ANALYSIS

Independent claim 1 recites in relevant part upon verifying that a first wrapped realized logic portion of a logic model design is functioning correctly, verifying the functionality of the wrapper associated therewith. Consistent with Appellants' Specification, we have reasonably but broadly construed the verification of the functionality of the wrapper to mean that compared data are identical or substantially similar. (Spec. 9-10.)

As detailed in the Findings of Facts section Okazaki teaches a dividing unit for partitioning design data on a logical circuit into LSI data and PGA connection data that are mapped into programmable chips to thereby generate an equivalent circuit. (FF. 1.) One of ordinary skill in the art would readily recognize that by performing an operation upon the design data to generate the LSI data mapped unto an equivalent logical circuit, Okazaki reasonably suggests a realization of the design data. Further, Okazaki teaches comparing the modified LSI data with the non-modified LSI data to determine whether to implement a logically changed circuit. (FF. 2.) The ordinarily skilled artisan would appreciate that by comparing the non-modified LSI data with the modified LSI data, Okazaki fairly suggests applying a wrapper to the non-modified LSI data to determine whether a

logical circuit corresponding thereto can be modified. Additionally, Okazaki teaches upon determining that it is feasible to modify the logical circuit, the corresponding LSI data is modified to thereby implement the circuit. (FF. 3.) The ordinarily skilled artisan would appreciate that, by first confirming that changes to the circuit are feasible before actually modifying the LSI data, Okazaki reasonably suggests verifying that the modified LSI data can function correctly before allowing the non-modified LSI data corresponding to the logical circuit to be updated.

We note however, that while the determination of the modification feasibility is based upon the result of the comparison between modified LSI data and non-modified LSI data, Okazaki's disclosure is silent on whether the compared data are found to be identical or substantially similar. We therefore find that Okazaki's disclosure does not particularly lend itself to verifying the functionality of a corresponding wrapper upon determining that the modification to an associated logical circuit is feasible. We thus agree with Appellants that Okazaki's disclosure falls short of suggesting or teaching verifying the functionality of a first wrapper upon verifying that a first wrapped realized logic portion of a logic model design is functioning correctly, as recited in independent claims 1, 11, 21, 31, and 33. We further agree with Appellants that Abts does not cure Okazaki's deficiencies. It follows that Appellants have shown that the Examiner erred in concluding that the combination of Okazaki and Abts renders claims 1 through 36 unpatentable.

VI. CONCLUSION OF LAW

Appellants have shown that the Examiner erred in concluding that the combination of Okazaki and Abts renders claims 1 through 36 unpatentable under 35 U.S.C. § 103(a).

VII. DECISION

We reverse the Examiner's decision rejecting claims 1 through 36 as being unpatentable under 35 U.S.C. § 103(a) .

REVERSED

msc

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