UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LARRY KIRN

Appeal 2008-5296
Application 10/649,218
Technology Center 2800

Decided: December 22, 2008

Before KENNETH W. HAIRSTON, JOHN A. JEFFERY, and CARLA M. KRIVAK, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellant appeals under 35 U.S.C. § 134 from the Examiner's rejection of claims 1-3. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

STATEMENT OF THE CASE

Appellant invented a method for asynchronous data demodulation using pulse width measurement based on an asynchronous clock. The demodulation method includes locking onto the data stream in accordance with measured pulse width, rather than inferred frequency.[1] Claim 1 is illustrative:

1. A method of demodulating a pulsewidth-modulated data stream using an asynchronous clock, comprising the steps of:

measuring a temporal aspect of the asynchronous clock; and

locking onto the data stream in accordance with the measured periods.

The Examiner relies on the following prior art references to show unpatentability:

Barnes	US 3,760,412	Sept. 18, 1973
Wagner	US 4,065,765	Dec. 27, 1977

1. The Examiner rejected claim 1 under 35 U.S.C. § 102(b) as anticipated by Wagner (Ans. 3).
2. The Examiner rejected claims 1-3 under 35 U.S.C. § 102(b) as anticipated by Barnes (Ans. 4).

Rather than repeat the arguments of Appellant or the Examiner, we refer to the Brief and the Answer for their respective details. In this decision, we have considered only those arguments actually made by Appellant. Arguments which Appellant could have made but did not make

[1] *See generally* Spec. 1-2.

in the Brief have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

The Anticipation Rejection Over Wagner

Regarding the Examiner's anticipation rejection of claim 1 over Wagner, Appellant argues that Wagner fails to disclose measuring a temporal aspect of an asynchronous clock and using such a measurement to lock onto a data stream. According to Appellant, Wagner teaches synchronizing an index signal with data input that is derived from a rotating light source (Br. 2).

The Examiner equates the disclosed recorder clock signal as corresponding to "measuring a temporal aspect of the asynchronous clock" since Wagner's recorder clock signal has 36 pulses. These pulses, the Examiner contends, result from measuring the clock signal (Ans. 5). The Examiner adds that the input to output process using the recorder clock signal in the 36-bit shift registers 139, 141 corresponds to "locking onto the data stream in accordance with the measured periods" as claimed (*Id.*).

The issue before us, then, is as follows:

ISSUE

Has Appellant shown that the Examiner erred in finding Wagner anticipates claim 1 under § 102? The issue turns on whether Appellant has shown that the Examiner erred in finding:

(1) Wagner's 36-pulse clock signal corresponds to "measuring a temporal aspect of the asynchronous clock" as claimed, and

(2) Wagner's use of the recorder clock signal in conjunction with the shift registers corresponds to "locking onto the data stream in accordance with the measured periods" as claimed.

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence:

1. Wagner discloses a pulse-width demodulator and information storage device that uses a pair of asynchronous clocking systems. One clocking system controls the transmitted data, and the other controls a recorder and clocks out stored data to the recorder (Wagner, col. 1, ll. 63-67; col. 2, l. 52 - col. 3, l. 2).

2. External recorder 106 provides a recorder clock signal "C" comprising a series of 36 clock pulses. This recorder clock signal is applied to AND gates 133 and 137 which are connected to OR gates 145 and 143, respectively. The output of OR gate 143 is connected to the clock input "C" of shift register 139. Likewise, the output of OR gate 145 is connected to the clock input "C" of shift register 141 (Wagner, col. 5, ll. 53-66; Figs. 1A-1B).

3. Thus, when the recorder clock signal C is on, its 36 pulses are applied to the clock input of shift register 139. As a result, all of the binary data stored in this shift register is shifted out, and a group of 36 zeroes in series is shifted into this register (Wagner, col. 7, ll. 19-31).

4. Likewise, the 36 pulses of recorder clock signal C is applied to the clock input of shift register 141 which shifts out all of the binary data stored

in that shift register and shifts a group of 36 zeroes in series in that register (Wagner, col. 7, ll. 39-46).

PRINCIPLES OF LAW

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. *RCA Corp. v. Appl. Dig. Data Sys., Inc.*, 730 F.2d 1440, 1444 (Fed. Cir. 1984); *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554 (Fed. Cir. 1983).

ANALYSIS

We find no error in the Examiner's findings that Wagner fully meets claim 1. At the outset, we note that the scope and breadth of "measuring a temporal aspect of the asynchronous clock" as claimed does not preclude the functionality of Wagner's 36-pulse recorder clock signal. As we indicated in the Findings of Fact section above, this clock signal is asynchronous (FF 1). Second, we agree with the Examiner that the fact that the clock signal comprises a series of 36 pulses (FF 2) would involve measuring a temporal aspect of this series to ensure that the requisite number of pulses is transmitted.

We also find no error in the Examiner's position that Wagner's process of using the recorder clock signal with respect to the 36-bit shift registers 139, 141 fully meets "locking onto the data stream in accordance with the measured periods" as claimed. As we noted in the Findings of Fact section above, the 36 pulses of the recorder clock signal are used to shift out

binary data inputted and stored in both of these shift registers (FF 3-4). We see no reason why this functionality would not involve locking onto the data stream in accordance with the 36 bits of the recorder clock signal. Appellant's arguments pertaining to the index signal synchronized with the input data as not teaching an asynchronous clock (Br. 2) are not germane to the Examiner's interpretation of Wagner which relies on the temporal aspect of the recorder clock signal and its associated functionality. We find no error in this approach.

For the foregoing reasons, Appellant has not persuaded us of error in the Examiner's rejection of claim 1 based on Wagner. Therefore, we will sustain the Examiner's rejection of that claim.

The Anticipation Rejection Over Barnes

We next consider the Examiner's anticipation rejection of claims 1-3 over Barnes. The Examiner notes Barnes' circuitry includes an asynchronous clock 14 with frequency f_0. This clock signal is measured to produce a compensated clock signal F (i.e., f_0 or $f_0/2$) and therefore corresponds to measuring a temporal aspect of an asynchronous clock as claimed. The Examiner further notes that since this compensated clock signal is inputted to gates 28, 30 along with the data signal 10, the gates therefore lock onto the data stream in accordance with the compensated clock (Ans. 4-5).

Regarding representative claim 1,[2] Appellant does not dispute the Examiner's interpretation of Barnes regarding measuring a temporal aspect of an asynchronous clock, but rather argues that the functionality relied upon by the Examiner does not disclose locking onto a data stream as claimed (Br. 3).

The issue before us, then, is as follows:

ISSUE

Has Appellant shown that the Examiner erred in finding Barnes anticipates claim 1 under § 102? The issue turns on whether Appellant has shown that the Examiner erred in finding that the functionality of Barnes' circuit, which utilizes gates that use inputs from a compensated clock and a data stream, locks onto a data stream in accordance with the measured periods as claimed.

FINDINGS OF FACT

The record supports the additional following findings of fact (FF) by a preponderance of the evidence:

5. Barnes discloses a nonsynchronous binary demodulator that demodulates a binary signal of varying pulse rate input inputted to data terminal 10 (Barnes, Abstract; col. 3, ll. 11-18; Fig. 1).

6. Barnes' demodulator circuit comprises a source 14 of clock pulses at frequency f_0 which is inputted to count rate compensation gate 24 along

[2] Appellant argues claims 1-3 together as a group. *See* Br. 2-3. Accordingly, we select claim 1 as representative. *See* 37 C.F.R. § 41.37(c)(1)(vii).

with pulses at one-half this frequency ($f_0/2$) (Barnes, col. 3, ll. 27-30; col. 5, ll. 29-43; Fig. 1).

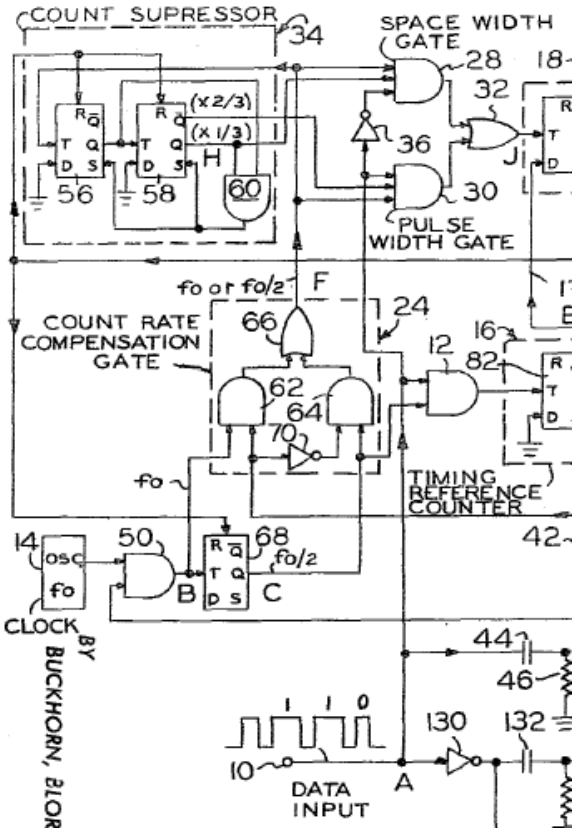
7. The compensated clock pulses F obtained from count rate compensation gate 24 are therefore equal to the frequency of the clock oscillator 14 frequency (f_0) or one-half that frequency ($f_0/2$) (Barnes, col. 5, ll. 40-50; Fig. 1).

8. The compensated clock pulses from compensation gate 24 are input to space width gate 28 and pulse width gate 30, respectively. The outputs of these gates are connected to the input of a comparator counter 18 via OR gate 32. This arrangement enables the counter to measure either the input pulse width or the space between pulses (Barnes, col. 4, ll. 12-20; Fig. 1).

9. Input pulses from data terminal 10 are input to the pulse width gate 30 directly and to the space width gate 28 via inverter 36. As such, gate 30 is turned on only during input pulses, and gate 28 is turned on only during spaces between input pulses (Barnes, col. 4, ll. 28-34; Fig. 1).

ANALYSIS

Based on the record before us, we find no error in the Examiner's position relying on the disclosure of Barnes as anticipating representative claim 1. For clarity, the relevant portion of Barnes' circuit in Figure 1 is reproduced below:



Relevant Detail Portion of Barnes' Circuit in Figure 1

As shown above, the compensated clock pulses F obtained from count rate compensation gate 24 are input to space width gate 28 and pulse width gate 30, respectively (FF 8). These pulses are equal to the frequency of the clock oscillator 14 frequency (f_0) or one-half that frequency ($f_0/2$) (FF 7). Ultimately, the outputs of these gates are connected to a comparator counter 18 (via OR gate 32) which enables the counter to measure either the input pulse width or the space between pulses (FF 8).

Based on this functionality, we see no error in the Examiner's position that the logic gates 28 and 30 lock the data stream in accordance with the

compensated clock F. Clearly, the compensated clock will dictate the functionality of not only the gates, but also the comparator counter connected thereto. Furthermore, input pulses from data terminal 10 are input to the pulse width gate 30 directly and to the space width gate 28 via inverter 36. As such, gate 30 is turned on only during input pulses, and gate 28 is turned on only during spaces between input pulses (FF 9). By virtue of this compensated clocking scheme with respect to the input data, we agree with the Examiner that Barnes' system locks onto the data stream in accordance with the measured periods as claimed.

For the foregoing reasons, Appellant has not persuaded us of error in the Examiner's rejection of representative claim 1. Therefore, we will sustain the Examiner's rejection of that claim, and claims 2 and 3 which fall with claim 1.

CONCLUSIONS OF LAW

Appellant has not shown that the Examiner erred in rejecting claim 1 over Wagner under § 102. Nor has Appellant shown that the Examiner erred in rejecting claims 1-3 over Barnes under § 102.

ORDER

The Examiner's decision rejecting claims 1-3 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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