

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MASAHIRO ARAKI
and CHIEKO HAYASHI

Appeal 2008-5457
Application 10/873,309
Technology Center 2800

Decided: December 11, 2008

Before KENNETH W. HAIRSTON, JOHN A. JEFFERY, and
THOMAS S. HAHN, *Administrative Patent Judges*.

HAHN, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134 from the Examiner's rejections of claims 5 and 6. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

STATEMENT OF THE CASE

Appellants invented improved spread spectrum clock generator circuitry capable of accurate frequency modulation. The invented circuitry includes first and second internal clock generator circuits. Both the first and second internal clock generator circuits utilize phase lock loop circuits. A first reference clock signal is input to a phase comparator circuit of the first internal clock generator. The phase comparator circuit also receives a first internal clock generator produced comparison clock signal, and the phase comparator outputs phase difference signals derived from the two compared input signals. The phase difference signals are processed and input as a control signal for a voltage controlled oscillation circuit that has a plurality of ring series inverters to output clock signals having different phases. The plurality of different phase clock signals is input to a selection circuit that also receives a signal from a first control circuit. The selection circuit utilizes the first control circuit signal to select and output a first oscillation clock signal. This first oscillation clock signal is input to a frequency divider circuit that outputs a second reference clock signal that is input to the second internal clock generator to produce an output oscillation clock signal.¹

Claim 5 is illustrative:

5. A spread spectrum clock generator, comprising:

a first internal clock generator generating a first oscillation clock signal obtained by multiplying a frequency of a first reference clock signal, based on received said first reference clock signal;

¹ See generally Spec. 14:20 – 15:14; Figs. 7 and 8.

a first frequency divider dividing a frequency of said first oscillation clock signal by a predetermined frequency division ratio so as to generate a second reference clock signal; and

a second internal clock generator generating a second oscillation clock signal obtained by multiplying a frequency of said second reference clock signal, in synchronization with said second reference clock signal; wherein

said first internal clock generator includes a phase comparator circuit comparing phases of said first reference clock signal and an internally generated comparison clock signal and outputting a phase difference signal in accordance with a comparison result,

an oscillation circuit generating a plurality of clock signals having different phases respectively based on said phase difference signal,

a second frequency divider dividing a frequency of any one clock signal among said plurality of clock signals from said oscillation circuit by a predetermined frequency division ratio so as to generate said comparison clock signal,

a selection circuit selecting any one of said plurality of clock signals from said oscillation circuit and outputting said first oscillation clock signal, and

a first control circuit controlling a selection operation of said selection circuit so as to modulate a frequency of said second oscillation clock signal.

The Examiner relies on the following prior art references to show unpatentability:

Nakatani	US 6,188,258 B1	Feb. 13, 2001
Wakayama	US 6,791,379 B1	Sep. 14, 2004 (filed Dec. 7, 1999)

Claims 5 and 6 stand rejected under 35 U.S.C. §103(a) as unpatentable over Nakatani and Wakayama (Ans. 3).

Rather than repeat the arguments of Appellants or of the Examiner, we refer to the Brief and the Answer² for their respective details. In this decision, we have considered only those arguments actually made by Appellants. Arguments that Appellants could have made but did not make in their Brief have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Appellants' Arguments

Appellants argue that both Nakatani and Wakayama teachings are deficient through asserting descriptions of how the references' disclosed circuitries operate. Appellants conclude by arguing that "the Examiner's asserted motivation [from Wakayama] to obtain a high-speed, low-jitter and high phase resolution circuit would not have realistically impelled a person skilled in the art to make the proposed [reference] combination" (emphasis deleted) (Br. 7), because this "motivation does not provide any reason why Nakatani's circuitry needs to be modified based on the teachings of Wakayama" (Br. 8).

² Appellants did not file a Reply Brief. We, therefore, refer to: (1) the Appeal Brief filed December 19, 2006, and (2) the Answer mailed April 18, 2007 throughout this opinion.

ISSUE

Have Appellants shown the Examiner erred in combining Nakatani and Wakayama teachings to arrive at the claimed invention? The issue turns on whether design incentives taught by Wakayama would prompt a skilled artisan to modify Nakatani with the circuitry disclosed in Wakayama.

FINDINGS OF FACT

The following Findings of Fact (FF) are supported by a preponderance of the evidence on the record before us:

1. Nakatani discloses clock signal generating circuitry that processes an input reference clock signal having a first frequency and outputs a second clock signal at a different frequency (Nakatani, Abstract; Fig. 1).
2. Nakatani clock signal generating circuitry includes a first frequency multiplier 11 interconnected by a frequency divider with a second frequency multiplier 18, and each of the frequency multipliers 11 and 18 includes a phase comparator (12 and 19) outputting signals that are processed to regulate voltage controlled oscillators (15 and 22) (Nakatani, col. 3, l. 49 -col. 6, l. 16; Fig. 1(reproduced below for reference)).

FIG.1

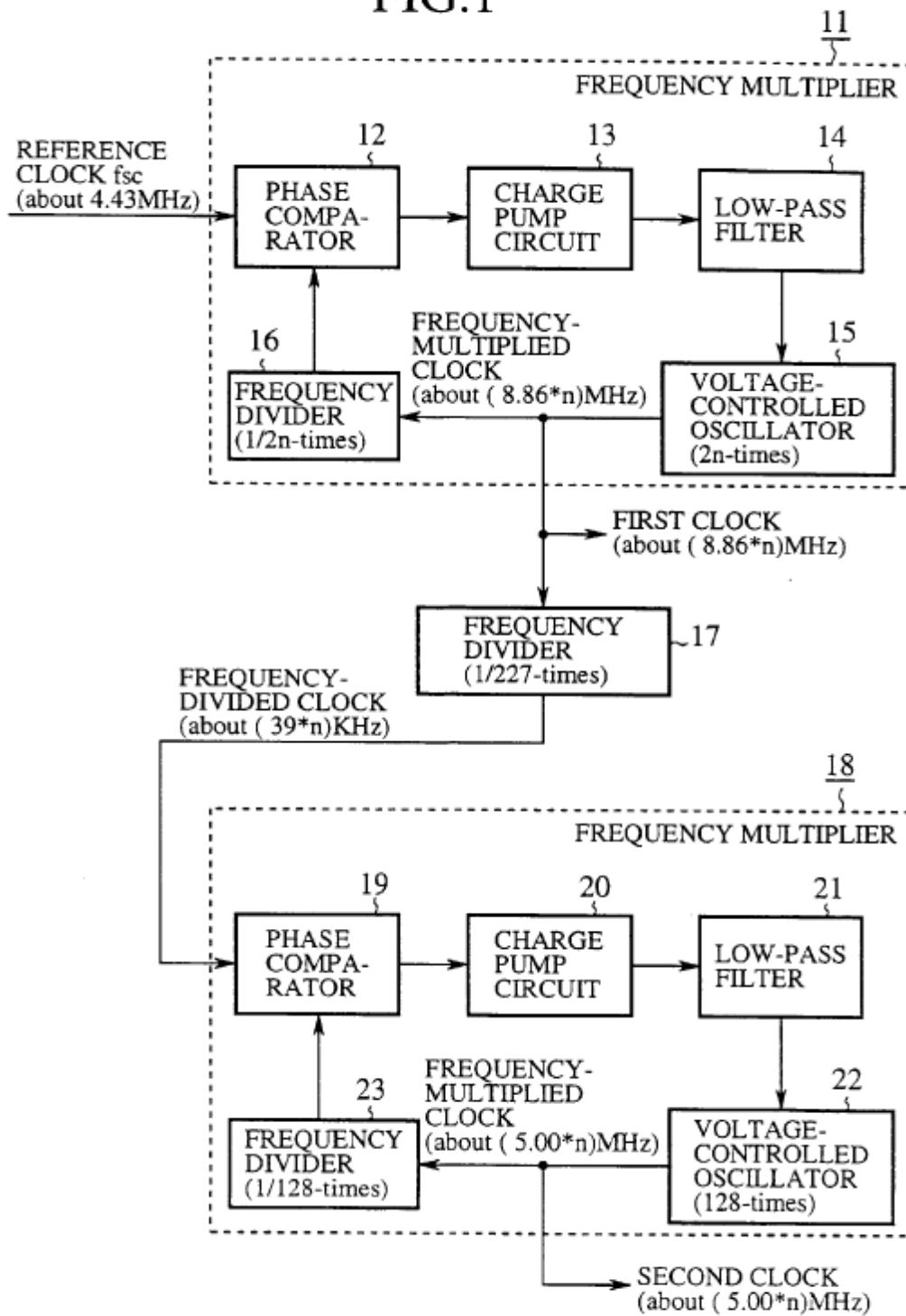


Figure 1 depicts a block diagram showing a Nakatani structure for a clock generating circuitry.

3. Wakayama discloses clock signal generating circuitry using a phase lock loop (PLL) circuit that processes an input reference clock signal having a first frequency and outputs a clock signal at a different frequency (Wakayama, col. 2, l. 44 – col. 3, l. 15; Fig 2).
4. The Wakayama clock signal generating circuitry includes a phase detector 10 outputting a signal that is processed to regulate a voltage controlled oscillator 14 which is configured to produce multi-phase clock signals that are input to a phase control MUX 18 along with a phase control signal “K” to have the phase control MUX 18 output a clock signal having a selected frequency and phase (Wakayama, col. 4, l. 51 – col. 5, l. 23; Fig. 2 (reproduced below for reference)).

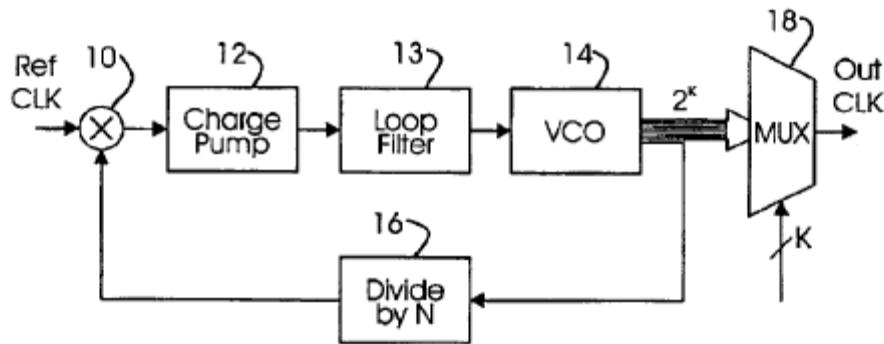


FIG. 2

Figure 2 depicts a block diagram showing a Wakayama structure for a multi-phase phase lock loop system.

5. Wakayama discloses that the PLL circuit provides “high-speed, low-jitter and high phase resolution” for clock signal generating circuitry (Wakayama, col. 2, ll. 44-48).
6. Wakayama teaches implementing a voltage controlled oscillator using a delay cell-based ring oscillator for outputting multi-phase clock signals (Wakayama, col. 6, ll. 8-11; Fig. 3).

PRINCIPLES OF LAW

An Examiner in rejecting claims under 35 U.S.C. § 103 must establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966).

The question of obviousness of claimed subject matter involving a combination of known elements is addressed in *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727 (2007), which explains:

When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida [v. AG Pro, Inc.]*, 425 U.S. 273 (1976) and *Anderson's-Black Rock[, Inc. v. Pavement Salvage Co.]*, 396 U.S. 57 (1969) are illustrative—a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

KSR, 127 S. Ct. at 1740.

When the Examiner's burden to establish a factual basis for supporting the conclusion of obviousness is met, the burden then shifts to the Appellants to overcome the Examiner's *prima facie* case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. *See In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

Non-obviousness arguments must address combined references as a whole and not separately consider the references without the combination being addressed. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986). "The test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art." *In re Young*, 927 F.2d 588, 591 (Fed. Cir. 1991) (internal citation omitted).

ANALYSIS

Obviousness Rejection over Nakatani, and Wakayama

Claim 5

The Examiner finds all limitations recited in independent claim 5 taught in Nakatani except for those covering "a selection circuit and a first control circuit" (Ans. 6). Appellants argue that Nakatani is deficient because Nakatani's circuitry is "directed to phase modulation by increasing the value

of n”³ (emphasis deleted) (Br. 7). The Examiner responds by “not[ing] that the claims … are structure claims, not claims describing the method or process of operation” (Ans. 10). Based on a preponderance of the evidence on the record before us, we concur in the Examiner’s findings that Nakatani teaches claim 5 recited elements (FF 1 and 2) except for those covering “a selection circuit and a first control circuit” (Ans. 6).

The Examiner turns to Wakayama and finds that “[t]he clock generator circuit of Wakayama discloses every element of the first clock generator claimed by the Appellants including the selection circuit and the first control circuit” (Ans. 9). The Examiner further finds that the Wakayama disclosed clock generator is taught as providing “a high-speed, low-jitter and high phase resolution circuit” (Ans. 5). The Examiner then reasons that “a person skilled in the art would have been motivated to substitute Wakayama’s [phase lock loop] PLL circuit for Nakatani’s PLL circuit in order to benefit from the advantages…” of high-speed, low-jitter and high phase resolution (Ans. 10). Appellants argue that Wakayama is deficient because Wakayama’s process is “directed to phase control by selecting one of a plurality of clock signals different from each other in phase” (emphasis deleted) (Br. 7).

We are not persuaded by Appellants’ arguments directed to processes taught by Nakatani and Wakayama, because as the Examiner indicates “the [appealed] claims … are structure claims, not claims describing the method or process of operation” (Ans. 10). Further, Appellants have not adequately

³ The value of “n” is a natural integer used to multiply a reference clock frequency (Nakatani, col. 3, ll. 7-8).

rebuted the Examiner's prima facie obviousness rejection by singularly attacking the Nakatani and Wakayama taught processes as opposed to addressing the combined reference teachings as a whole.⁴

Appellants additionally argue that:

The Examiner's asserted motivation does not provide any reason why Nakatani's circuitry needs to be modified based on the teachings of Wakayama. Therefore, the Examiner's asserted motivation to obtain a high-speed, low-jitter and high phase resolution circuit would not have realistically impelled a person skilled in the art to modify Nakatani's circuitry to make the proposed combination.

(Br. 8) We are not persuaded by Appellants' argument refuting combining references through modification, because references can be combined for a prima facie obviousness rejection without reasoning being derived from one reference to modify another's teachings. The Supreme Court, on this matter, explains: "When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one." *KSR*, 127 S. Ct. at 1740. The Nakatani and Wakayama teachings are in one field of endeavor, i.e., designs for clock signal generating circuitry (FF 1 and 3). Wakayama teaches design incentives of providing high-speed, low-jitter and high phase resolution for clock signal generating circuitry by use of the disclosed circuit (FF 5). Accordingly, we are persuaded the Examiner has set out a prima facie

⁴ "Non-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references." *Merck*, 800 F.2d at 1097 (internal citation omitted).

obviousness rejection in “not[ing] that a person skilled in the art would have been motivated to substitute Wakayama’s PLL circuit for Nkatani’s PLL circuit in order to benefit from the advantages...” (Ans. 10). Based on this record, we are also persuaded that Appellants have not persuasively rebutted the Examiner’s prima facie case of obviousness based on the collective teachings of the cited references.

For the foregoing reasons, Appellants have not persuaded us of error in the Examiner’s rejection of claim 5. Therefore, we will sustain the Examiner’s rejection of claim 5.

Claim 6

The Examiner finds the claim 6 recited structure elements being taught in Wakayama (Ans. 5-6). The entirety of Appellants’ non-obviousness arguments directed to claim 6 is (1) “neither Nakatani nor Wakayama teaches the [claim 6] additional requirements” (Br. 9), and (2) “the lack of disclosure in the applied references of all requirements of parent claim 5” (*Id.*).⁵ Appellants submit neither evidence nor argument beyond these stated conclusive assertions to address the Examiner’s prima facie case of obviousness for claim 6.

Once the Examiner satisfied the burden of presenting a prima facie case of obviousness, the burden shifted to Appellants to present evidence

⁵ In asserting that Nakatani and Wakayama fail to teach the claim 6 limitations, Appellants further argue that the claim 6 “requirements” have not “been addressed in the [final] Office Action [mailed August 4, 2006]” (Br. 9). We find the record contradicts this assertion, in that the Examiner addresses claim 6 recited subject matter with the same reasoning and rationale for the obviousness rejection in both the action (p. 5) and the Answer (Ans. 5-6). Appellants’ assertion is therefore not persuasive.

and/or arguments that persuasively rebut the Examiner's prima facie case. *See In re Oetiker*, 977 F.2d at 1445. Since we find Appellants do not particularly point out errors in the Examiner's reasoning to persuasively rebut the prima facie case of obviousness, we will sustain the rejection of claim 6.

CONCLUSION OF LAW

Appellants have not shown that the Examiner erred in combining the teachings of Nakatani and Wakayama, because Appellants have not shown the Examiner erred in finding that the design incentives in Wakayama would motivate a skilled artisan to modify Nakatani with the circuitry disclosed in Wakayama.

DECISION

We have sustained the Examiner's rejection with respect to all claims on appeal. Therefore, the Examiner's decision rejecting claims 5 and 6 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

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AFFIRMED

gvw

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