UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte BINAN WANG

Appeal 2008-5817
Application 10/921,001
Technology Center 2600

Decided: December 11, 2008

Before MAHSHID D. SAADAT, ROBERT E. NAPPI,
and KARL D. EASTHOM, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134 from the Examiner's Final Rejection of claims 21-28. No other claims are pending (Br. 2-3; Ans. 2).[1] We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Appellant discloses and claims an integrated circuit having a clock generator 16. The clock generator 16 delays a clock signal input to the generator in varying degrees, creating a plurality of delayed clock outputs 22. The delayed outputs, except the last, which is delayed by one full input clock cycle, are skewed relative to the input (*see* Fig. 7). In one embodiment (Fig. 8A), the clock generator delayed output 22 clocks an analog circuit 18, while the clock generator input clocks a digital circuit 17. In another embodiment (Fig. 8B), the opposite occurs. The clock generator delayed output creates clocks a digital circuit 17, while the clock generator input clocks an analog circuit 19. (Spec. 8: 4-19; 18: 2-9). Skewing the generator clock output relative to the generator clock input decreases degradation due to noise (*see* Spec. 5: 2-6; 19:9-11; 20:2-4).

Claim 21, illustrative of the invention, follows:

21. A mixed signal integrated circuit, comprising:

(a) a digital circuit with a digital clock signal input;

(b) an analog circuit with an analog clock signal input; and

(c) an analog clock generator with a generator input coupled to said digital clock signal input and with a generator output coupled to said analog clock

[1] The Examiner's Answer (mailed October 10, 2007) ("Ans.") and Appeal Brief (filed, July 7, 2007) ("Br.") detail the parties' positions.

signal input, said generator including a delay-locked-loop with said generator output connected to one of a plurality of delay cells of said delay-locked-loop;

(d) wherein an analog clock signal at said generator output is skewed from a digital clock signal at said generator input.

The Examiner relies on the following prior art reference to show unpatentability:

Lu	US 6,100,735	Aug. 8, 2000

The Examiner rejected claims 21 through 28 under 35 U.S.C. § 103(a) as being obvious based on Lu.

ISSUE

Appellant contends that Lu does not teach an analog clock and a digital clock with a skew between them as claims 21-28 require (Br. 5). The Examiner found all the disputed limitations obvious over Lu. (Ans. 3-4). Appellant groups claims 21-22 and 25-26 together, and claims 23-24 and 27-28 together. Accordingly, we select independent claims 21 and 23 as representative of the two groups.

The issue: Did Appellant demonstrate that the Examiner erred in finding that it would have been obvious to time both a digital and an analog circuit with Lu's clock as set forth in claims 21 and 23?

FINDINGS OF FACT (FF)

1. Appellant admits that a known skewing technique, depicted in Appellant's Figure 3, includes generating a delayed analog clock signal from an input digital clock signal:

> Another known technique for avoiding the above-mentioned degradation of analog circuit performance due to digital noise coupling is to use simple delay cells to skew the analog clock signal with respect to the digital clock signal. Fig. 3 illustrates such a simple delay cell. . . . A digital clock signal IN is applied to the input of inverter 11-1, and the delayed or skewed analog output clock signal OUT is produced at the output of inverter 11-2. Unfortunately, the delay times of such simple delay cells are very dependent on integrated circuit chip temperature variations, semiconductor manufacturing process variations, and power supply variations, and therefore tend to be quite inaccurate.

(Spec. 4: 13 to 5:1, Fig. 3).

2. Appellant also admits that another known similar skewing technique includes generating a digital clock signal from a delayed analog clock signal. (Spec. 3: 13-17).

3. Lu discloses a precise prior art clock (Fig. 1) having 128 selectable delayed outputs, relative to a master clock input. Each delayed output, except the last, is out of phase with the clock input. The last output is in phase with the input. (Lu, col. 1, l. 36 to col. 2, l. 35; Fig. 1). Lu's clock (Figs. 3, 11) improves on the prior art clock, providing a temperature and process independent precision clock with less parts and the same number of selectable delayed outputs. (Lu, col. 10, ll. 20-56).

4. Lu discloses that many "telecom" applications require such precise clocks. For example, transmitter digital to analog and receiver analog to digital converters require precise clocks (col. 1, ll. 11-17).

5. The Examiner found that modifying Lu would have been obvious

> . . . since the clock generator of Lu is seen as an intermediate device of a telecommunication system to provide various clocks (i.e., outputs of clock generator) from a master clock (i.e., input of a clock generator) for various component[s] within the system. Therefore, having digital/analog device(s) coupled to input/output of the clock generator is considered as an intended use of the clock generator.

(Ans. 3).

6. Appellant's response to the Examiner's findings follows:

> The claims require both an analog clock and a digital clock with the analog clock generated from the digital clock but skewed from it. In contrast, FIG. 1 of Lu shows a clock generator including a delay-locked loop (DLL) but nothing further. Lu has no suggestion of both digital and analog clocks with a skew between them; rather, Lu discloses clock division with a few delay cells in a DLL.

(Br. 5).

PRINCIPLES OF LAW

"[T]here must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006). "On appeal to the Board, an applicant can overcome a rejection by showing insufficient evidence of *prima facie* obviousness . . . ." *Kahn*, 441 at 985-86 (Fed. Cir. 2006) (*quoting In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998).

> If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same

> reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

KSR Int'l Co. v. Teleflex, Inc., 127 S.Ct. 1727, 1740 (U.S. 2007).

"[W]hen a patent 'simply arranges old elements with each performing the same function it had been known to perform' and yields no more than one would expect from such an arrangement, the combination is obvious." *Id.*, at 1740 (*quoting Sakraida v. Ag. Pro. Inc.*, 425 U.S. 273, 282 (1976)).

"Under the correct analysis, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed." *Id.*, at 1742.

ANALYSIS

Appellant's claimed invention, as recited in claim 21, amounts to a digital circuit clocked by Lu's input master clock, and an analog circuit clocked by Lu's clock generator output. Appellant does not challenge with any specificity, the Examiner's general finding that Lu's clock generator, as viewed by ordinarily skilled artisans, constitutes an intermediate telecommunications device that clocks both analog and digital circuits with whatever clock signal the circuits require, such as Lu's master clock input or one of Lu's selectable delayed outputs. (*See* FF 5, 6).

Lu supports the Examiner's findings (FF 3, 4). Lu reasonably teaches clocking any type of telecommunications circuit, such as analog to digital, or digital to analog, converters, with any one of the precise delayed clock

generator outputs. Lu also reasonably suggests clocking any such circuit not requiring a precise delay with the master input clock. Lu's clock simply provides an array of clock choices, delayed or skewed at one of the many selectable outputs, and non-delayed at the clock generator input. (*See* FF 3, 4).

Further, Appellant admits that known techniques included, as the Examiner generally found in relation to Lu's clock, connecting an analog circuit to a clock generator output while at the same time connecting a digital circuit to a master clock input (*see* FF 1). Appellant also admits known techniques included a reversed version of the output and input connections, i.e., creating a delayed digital clock from the master input analog clock (*see* FF 2). As the Examiner also generally found (Ans. 3), it would have been obvious to clock either analog or digital telecommunications circuits at either Lu's input or one of Lu's skewed outputs, because Lu's clock provides various precise clock choices for a variety of telecommunications circuits.

According to Appellant, prior art clock skewing arrangements also were known to provide noise suppression; however they were also known to lack accuracy. (FF 1, 2). Lu's delay clocks provide a number of selectable and accurate delayed clock signals, thereby solving the known problem of inaccuracy confronting skilled artisans (FF 3, 4) and providing further motivation to use the clocks in known circuits (*see* FF 1, 2). *See KSR*, *supra*. That is, substituting Lu's clock generator (FF 3) in place of the admitted prior art clock generators (FF 1, 2), using one of the 128 selectable skewed outputs, also meets claims 21 and 23. A person of ordinary skill in

the art would have recognized that Lu's prior art clock technique would have improved the similar admitted prior art circuits in the same way. *See Id*.

Alternatively viewed, connecting a known analog circuit to one of the 128 precision clock outputs of Lu's clock, while connecting a known digital circuit to the input master clock, as required by claim 21, amounts to the predictable beneficial use of prior art techniques to eliminate noise and provide precise timing. Similarly, interchanging the analog and the digital circuits, as generally required by claim 23 relative to claim 21, amounts to the same predictable beneficial use of prior art techniques. Following *KSR*, 127 S.Ct. at 1740 (*quoting Sakraida*), *supra*, each claimed combination "'simply arranges old elements with each performing the same function it had been known to perform' and yields no more than one would expect from such an arrangement, [and therefore] the combination is obvious."

Contrary to Appellant's further argument (*see* FF 6) that Lu's outputs are not skewed relative to the input, each of Lu's selectable outputs, except the final output, are delayed (i.e., skewed) relative to the input, as the Examiner generally found. (Ans. 3-6, FF 3). Therefore, Lu meets element (d) recited in claims 21 and 23, as the Examiner also generally found (Ans. 3-6).

SUMMARY

Appellant fails, under *Kahn*, to demonstrate error in the Examiner's findings. Specifically, Appellant did not demonstrate that the Examiner erred in finding that it would have been obvious to time both a digital and an analog circuit with Lu's clock as set forth in independent claims 21 and 23. We sustain the 35 U.S.C. § 103 rejection of claims 21-28.

DECISION

The Examiner's decision rejecting claims 21-28 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv)(2006).

AFFIRMED

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