

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte GUSTAVO J. MEHAS,
CHUN CHEUNG,
and BRANDON D. DAY

Appeal 2008-6342
Application 10/917,628
Technology Center 2800

Decided: January 14, 2009

Before KENNETH W. HAIRSTON, JOHN A. JEFFERY, and
THOMAS S. HAHN, *Administrative Patent Judges*.

HAHN, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134 from the Examiner's rejections of claims 7, 9, 11, 12, and 15-24. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

STATEMENT OF THE CASE

Appellants invented a comparator based hysteresis control circuit for enabling an external circuit, e.g., a DC-DC voltage converter. The control circuit includes an enable pin that is connected to an external voltage signal. The enable pin is also connected to an input of a comparator, and a reference voltage is connected to another input of the comparator. Additionally connected to the enable pin is a current source that can act as a current sink. The current source is further connected to an output of the comparator. When the external voltage signal exceeds the reference voltage, the comparator outputs a first signal level that deactivates the current source and activates a connected external circuit. When the external voltage signal is less than the reference voltage, the comparator outputs a second signal level that activates the current source and deactivates the connected external circuit. The comparator output signals may be used for functions other than enablement of a DC-DC converter, such as voltage monitoring and activation of test/trim modes.¹ Claim 7 is illustrative. The disputed limitation is emphasized for clarity:

7. A DC-DC voltage converter package comprising:

a DC-DC voltage converter circuitry;

an enable pin for receiving an external voltage signal to enable and disable the DC-DC voltage converter circuitry responsive to the external voltage signal;

a current sink connected to the enable pin within the DC-DC voltage converter package for providing hysteresis control on the enable pin

¹ See generally Spec. ¶¶ 0009-0015; Figs. 1 and 2.

of the DC-DC voltage converter circuitry; and

a comparator within the DC-DC voltage converter package for comparing the external voltage signal to a reference voltage signal, wherein the comparator generates a control signal at a first voltage level for disabling the current sink and enabling the DC-DC voltage converter circuitry if the input voltage signal is greater than the reference voltage signal and generates the control signal at a second voltage level for enabling the current sink and disabling the DC-DC voltage converter circuitry if the input voltage signal is less than the reference signal, wherein *the enable pin is used for an alternate function when the DC-DC voltage converter circuitry is disabled.*

The Examiner relies on the following prior art references to show unpatentability:

Shacter	US 6,316,978 B1	Nov. 13, 2001
Yoshimura	US 2003/0202379 A1	Oct. 30, 2003

Claims 7, 9, 11, 12, and 15-24 stand rejected under 35 U.S.C. §103(a) as unpatentable over Yoshimura and Shacter (Ans. 3).

Rather than repeat the arguments of Appellants or of the Examiner, we refer to the Brief and the Answer² for their respective details. In this decision, we have considered only those arguments actually made by Appellants. Arguments that Appellants could have made but did not make in their Brief have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

² Appellants did not file a Reply Brief. We, therefore, refer to (1) the Appeal Brief filed June 22, 2007, and (2) the Answer mailed October 10, 2007 throughout this opinion.

Appellants' Arguments

Appellants do not separately argue the individual claims within the rejection. Instead, Appellants address appealed independent claims 7, 11, and 15 by asserting that:

Claims 11 and 15 include limitations similar to those of Claim 1 [sic] and are allowable over the recited combination of the *Yoshimura* and *Shacter* since the Examiner has failed to establish a *prima facie* case as to why these combination of references teach all of the limitations of claims 11 and 15 for reasons similar to those discussed with respect to Claim 1 [sic].³

(Br. 16). With respect to the remaining appealed claims the Appellants assert “the Examiner has improperly applied the *Yoshimura* and *Shacter* references to Claims 7, 9, 11-13 [sic] and 15-24” (Br. 5).⁴ We, accordingly, select claim 7 as representative. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Appellants' arguments are that (1) “the various combinations of references proposed by the Examiner are not supported by a proper suggestion or motivation to make each proposed modification” (Br. 6), and (2) “[t]he Examiner has provided no discussion that the *Shacter* reference either explicitly or implicitly describes that the enable pin could be used for some alternative function” (Br. 15).

³ Claim 1 is a canceled claim (Br. 17). We, therefore, presume Appellants' listing of claim 1 is a typographical error, and also presume, based on the record that Appellants intended to list independent claim 7 as the claim including limitations similar to claims 11 and 15.

⁴ Claim 13 is canceled (Br. 18).

ISSUE

Have Appellants shown the Examiner erred in combining the teachings of Yoshimura and Shacter to arrive at the claimed invention? The issue turns on whether (1) the Examiner provides reasoning and rationale for combining the references, and (2) Shacter teaches or suggests using a comparator based hysteresis control circuit for alternative functions.

FINDINGS OF FACT

The record supports the following Findings of Fact (FF) by a preponderance of the evidence:

1. Yoshimura discloses an electronic circuit including an external power source with a connected voltage regulator controlled by a comparator based enablement circuit (Yoshimura, ¶¶ 0026-0030; Fig. 3).
2. Shacter teaches a comparator based circuit that is disclosed as providing hysteresis control independent of process, temperature, and supply voltage variations (Shacter, Abstract; col. 1, ll. 10-14).
3. Shacter discloses a hysteresis control circuit that includes a node connected to an input voltage and a comparator for determining reference and input voltage differences and outputting signal values to a current source also connected to the node, so that the current source outputs a first current level to the node when the comparator outputs a first value signal and the current source outputs a second current level to the node when the comparator outputs a second value signal (Shacter, col. 3, l. 30 – col. 4, l. 9; Fig. 2).

PRINCIPLES OF LAW

An Examiner in rejecting claims under 35 U.S.C. § 103 must establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). Among the factual determinations is a requirement to ascertain differences between prior art and claims at issue (*Id.*). When claims in issue cover an apparatus, the claimed elements can be defined structurally or functionally, i.e., by what the element does. *In re Schreiber*, 128 F.3d 1473, 1478 (Fed. Cir. 1997). Even though an apparatus may be claimed either structurally or functionally, a claimed apparatus is only distinguishable from prior art in terms of structure not function. *Id.* at 1477-78. “[A]pparatus claims cover what a device is, not what a device does.” *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1468 (Fed. Cir. 1990) (emphasis deleted).

The question of obviousness of claimed subject matter involving a combination of known elements is addressed in *KSR Int’l v. Teleflex, Inc.*, 127 S. Ct. 1727 (2007), which explains:

When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida [v. AG Pro, Inc.]*, 425 U.S. 273 (1976)] and *Anderson's-Black Rock[, Inc. v. Pavement Salvage Co.]*, 396 U.S. 57 (1969)] are

illustrative—a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

KSR, 127 S. Ct. at 1740.

If the claimed subject matter cannot be fairly characterized as involving the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement, a holding of obviousness can be based on a showing that “there was an apparent reason to combine the known elements in the fashion claimed.” *Id.* at 1740-41. Such a showing requires

some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

Id. at 1741 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)) (internal quotation marks omitted).

During examination of a patent application, a claim is given its broadest reasonable construction “in light of the specification as it would be interpreted by one of ordinary skill in the art.” *In re Am. Acad. Of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004).

ANALYSIS

We begin our analysis with Appellants’ argument that the Examiner’s combining of Yoshimura and Shacter is “not supported by a proper suggestion or motivation to make each proposed modification” (Br. 6). The

Examiner's indicated modification is "to use Shacter's enable circuit for Yoshimura's [sic] enable circuit 10 ..." (Ans. 3). The Shacter enable circuit that the Examiner indicates for modifying Yoshimura with is shown in Shacter Figure 2 that is reproduced below:

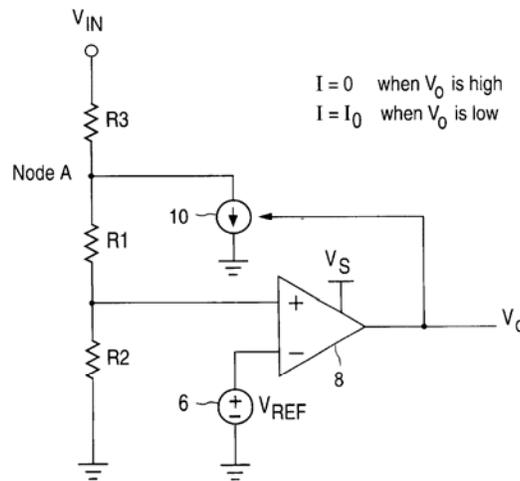


FIG. 2

**Figure 2 of Shacter Showing Schematic Drawing of
Comparator 8 Based Enablement Circuit**

The Yoshimura enable circuit 10 that the Examiner indicates for modification with the Shacter enable circuit is shown in Yoshimura Figure 3 that is reproduced below:

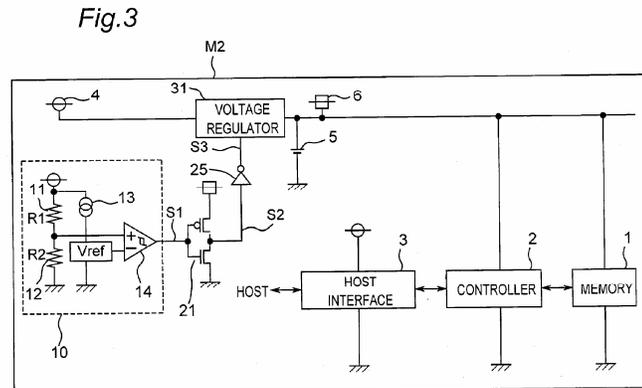


Figure 3 of Yoshimura Showing Block and Schematic Drawing of a Circuit Including Voltage Regulator 31 with Enable Circuit 10

We noted above in the Findings of Fact section that Shacter teaches a comparator based enable circuit to provide hysteresis control with disclosed advantages of being independent of process, temperature, and supply voltage variations (FF 2). We are persuaded that the Examiner in relying on the Shacter disclosures of advantages has set out a prima facie obviousness rejection by reasoning that “Shacter’s figure 2 shows an enable circuit having the advantage of being independent of temperature and process variations” (Ans. 3). Referencing these advantages, the Examiner, for example, reasons that “it would have been obvious to one having ordinary skill in the art to use Shacter’s enable circuit for Yashimura’s [sic] enable circuit 10 for the purpose of reducing circuit dependence on temperature and process variations, thereby improving the circuit performance” (*Id.*). Responding to Appellants’ assertion that the combined reference

obviousness rejection lacks adequate motivation, the Examiner repeats the reasoning reproduced here for combining references, and further notes that Appellants provide “no specific argument to why the Yashimura [sic] and Shacter references are not combinable” (Ans. 5). Appellants are silent as the Examiner notes. Accordingly, Appellants have not persuaded us of error in the Examiner’s articulated reasoning and rational underpinning for the combination of references that support the prima facie obviousness rejection.

Continuing, we note that Appellants do not dispute the Examiner’s findings regarding Yoshimura teaching a DC-DC converter package including DC-DC converter circuitry with an enabling circuit (Ans. 3). Rather, Appellants argue that “[t]he Examiner has provided no discussion that the *Shacter* reference either explicitly or implicitly describes that the enable pin could be used for some alternative function” (Br. 15). The claim 7 recited limitation that Appellants rely on reads: “the enable pin is used for an alternative function when the DC-DC voltage converter circuitry is disabled.”

The Examiner responds to Appellants’ argument by noting that:

The limitation “is used for” is clearly seen as an intended use limitation. Scharter’s [sic] circuit figure 2 is capable of being used for alternative function or any required function when the DC-DC converter circuitry is disabled, so indeed the circuit is available to be used for any other particular function.

(Ans. 5). Given that the recited limitation does not identify a specific alternative function, we find no error in the Examiner indicating that the Shacter taught circuit is “available to be used for any other

particular function” (*Id.*). The Examiner is broadly interpreting the claim, and it is the broadest reasonable construction that is required to be given to an examined claim. *Am. Acad. Of Sci. Tech. Ctr.*, 367 F.3d at 1364. Appellants do not argue that Shacter teaches or suggests any restriction as to any functions that can be enabled with the disclosed circuit. Therefore, we concur with the Examiner that the scope and breadth of the recited limitation encompasses any function for which the Shacter enable circuit could be used.

We also are not persuaded by the Appellants’ alternative function argument, because “apparatus claims cover what a device is, not what a device does.” *Hewlett-Packard Co.*, 909 F.2d at 1468 (emphasis deleted). Appellants assert that Shacter is deficient based on arguments concerning an unspecified function, not structure.⁵ The claimed enable pin in conjunction with the recited control signal is recited “to enable and disable the DC-DC voltage converter circuitry,” but no structure to accomplish functions other than enablement and disablement is recited. In any event, we see no reason why Shacter teachings would not be encompassed by the recited “some alternative function[s],” particularly in view of the Shacter taught control circuit providing different value output signals that are without restricting disclosure as to what functions could be enabled. While Shacter is silent as to what functions can be enabled by the comparator output signals, we

⁵ The disputed limitations in the appealed claims are not in means-plus-function format and, therefore, do not incorporate Specification-disclosed or equivalent structures as authorized by 35 U.S.C. § 112, sixth paragraph. *See In re Morris*, 127 F.3d 1048, 1055 (Fed. Cir. 1997) (“There is no comparable mandate in the patent statute that relates the claim scope of non-§ 112 ¶ 6 claims to particular matter found in the specification.”).

concur with the Examiner that skilled artisans would nonetheless recognize that the comparator output signals would be capable of enabling “alternative function[s]” as is claimed (Ans. 4 and 5). As such, we see no reason why Shacter teachings would be incapable of enabling control for the recited “alternative function.” On the record before us, we therefore find that Appellants have not persuasively rebutted the Examiner’s prima facie obviousness rejection.

For the foregoing reasons, Appellants have not persuaded us of error in the Examiner’s rejection of representative claim 7. Therefore, we will sustain the Examiner’s rejection of that claim, and claims 9, 11, 12, and 15-24 that fall with claim 7.

CONCLUSIONS OF LAW

Appellants have not shown that the Examiner erred in combining Yoshimura and Shacter for the prima facie obviousness rejection under § 103, because Appellants have not shown the Examiner erred in (1) the reasoning and rationale for the combination of references obviousness rejection, and (2) finding Shacter teaches or suggest using a comparator based hysteresis control circuit for alternative functions.

DECISION

We have sustained the Examiner’s rejection with respect to all claims on appeal. Therefore, the Examiner’s decision rejecting claims 7, 9, 11, 12, and 15-24 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

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AFFIRMED

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