

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

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Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte TOMOKI NISHINO

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Appeal No. 96-0523  
Application 07/910,763<sup>1</sup>

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HEARD: January 12, 1998

Before BARRETT, LEE, and TORCZON, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

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<sup>1</sup> Application for patent filed July 8, 1992, entitled "Semiconductor Wafer," which claims the foreign priority benefit under 35 U.S.C. § 119 of Japanese Application 3-178372, filed July 18, 1991. Counsel for appellant indicated at the oral hearing that there are no related appeals and that Sony Corporation is the real party in interest.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-12, all of the claims pending in the application. The amendment after final rejection received October 27, 1994, has not been entered.

We affirm-in-part.

The disclosed invention is directed to a method and apparatus for applying test signals or voltage to integrated circuit chips while the chips are still part of the wafer.

Claim 1 is reproduced below.

1. A semiconductor wafer, comprising:

a plurality of semiconductor chips formed in said semiconductor wafer;

a pair of supply and ground pad electrodes formed on each of said semiconductor chips;

a pair of external supply and ground terminal electrode pads formed on an outer peripheral portion of said semiconductor wafer; and

a power supply bus line and a ground bus line which are made of the same material as said pad electrodes, which are formed on said semiconductor wafer and which respectively interconnect said external supply and ground terminal electrode pads and each of said supply and ground pad electrodes on each of said semiconductor chips for simultaneously supplying an identical signal or voltage to all of said semiconductor chips on said semiconductor wafer.

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The examiner relies upon the following prior art:

|                          |           |                  |
|--------------------------|-----------|------------------|
| Quinn et al. (Quinn)     | 4,722,060 | January 26, 1988 |
| Stopper et al. (Stopper) | 4,847,732 | July 11, 1989    |

Claims 1-12 stand rejected under 35 U.S.C. § 103 as being unpatentable over Stopper and Quinn.

We refer to the Examiner's Answer (Paper No. 15) for a statement of the examiner's position and to the Appeal Brief (Paper No. 14) and the Reply Brief (Paper No. 17) for a statement of appellant's position.

#### OPINION

##### Grouping of claims

It is not clear exactly what the examiner means by the discussion under the "Grouping of claims" (Examiner's Answer, page 2). The examiner does not state, for example, what claims are presumed to stand or fall together or point out how the claims have not been separately argued. For the reasons stated the Reply Brief, the claims cannot be considered to stand or fall together, but must be considered individually, although there is parallelism between the claims that simplifies the analysis.

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Claims 1, 6-8, 11, and 12

Only Stopper is required in the rejection of independent claims 1, 8, and 12 and dependent claims 6, 7, and 11. Quinn is cited by the examiner for the teachings of a fuse and for forming semiconductor chips by cutting up the wafer; however, these limitations are not present in the independent claims.

Stopper discloses that the "real estate of the wafer is divided into special areas called cells and signal hookup areas and power hookup areas are provided" (col. 6, lines 10-12). The wafer has "active die incorporated on it, which die are isolated one from the other, and which each have die contact sites 202 normally used for probing during testing and for bonding during packaging" (col. 6, lines 21-24). "The wafer has a plurality of VLSI die manufactured in accordance with the present state of the art technology. These die are illustrated as 256K ram chips are capable of being manufactured by standard processes on a single wafer." Col. 7, lines 32-36. The individual die which occupy the cells in Stopper are "semiconductor chips" and therefore Stopper has "a plurality of semiconductor chips formed in said semiconductor wafer," as recited in claims 1 and 8, and

"a plurality of semiconductor chips . . . on a single wafer," as recited in the preamble of claim 12. None of the independent claims require that the wafer be cut into individual die and so appellant's arguments that Stopper teaches away from cutting the wafer into individual die (Brief, pages 5-6) are not persuasive because they are not commensurate in scope with the claims.

Figures 4 and 5 of Stopper show a power grid 11 with a rail system. "In a rail system, each cell is crossed by both rails three times in both the horizontal and vertical directions. The power rails are connected to a pair of contact pads 12 in each power hookup area 5." Col. 4, lines 7-10. "[T]he power hookup areas may be provided in the space at the 'corners.'" Col. 4, lines 64-65. The two rails in Stopper constitute "a power supply bus line and a ground bus line" as recited in claim 1 and "a power supply bus line means and a ground bus line means" as recited in claims 8 and 12. The pair of contact pads in the power hookup area 5 at the corners which are connected to the rails are "external supply and ground terminal electrode pads formed on an outer peripheral portion of said semiconductor wafer," as recited in

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claims 1 and 8 and are "external supply and ground terminal electrode pads on an outer peripheral portion of said semiconductor wafer," as recited in claim 12. Stopper shows power grid bonding pads 8 at the edge of the chip in figure 5 (col. 4, line 12; col. 12, approx. lines 29-37, discussing putting pads for voltage and ground at the side of the chip) which are "supply and ground pad electrodes" on each of the die. Stopper does not expressly show the power grid connected to voltage and ground pad electrodes on the individual chips; however, it would have been obvious to one of ordinary skill in the art to interconnect the rails of the power grid to the voltage and ground pad electrodes because that is the way power is supplied to the chip.

Because the two rail power grid connects all of the individual die on the wafer together, see figure 4, the grid is used "for simultaneously supplying an identical signal or voltage to all of said semiconductor chips on said semiconductor wafer," as recited in claim 1. Appellant argues "that neither of Stopper et al. nor Quinn et al. provide an arrangement via which the very same voltage or signal could be simultaneously supplied to each of die or chip on the wafer in

a manner to test the status of the circuitry in each of the dies or chips, after the chips had been exposed to a burn-in test or the like" (Brief, page 10). However, claim 1 requires only supplying an identical voltage to all the semiconductor chips, which is performed by the power grid in Stopper. Claim 1 does not require testing. Appellant has not persuaded us that the language of claim 1 defines over Stopper. The rejection of claim 1 is sustained.

Stopper states that "the power hookup areas may be provided in the space at the 'corners'" (col. 4, lines 64-65; see the power hookup area 5 in figure 4). Therefore, Stopper discloses placing the external terminal electrode pads in an isolated peripheral area of the wafer as recited in claim 6. Appellant's argument that neither of the references can be relied on to teach such a remote arrangement (Brief, page 14) is not persuasive because it does not address the clear teachings of Stopper. The rejection of claim 6 is sustained.

Figures 4 and 5 of Stopper show the power supply and ground grids crossing over each other. It would have been apparent to one of ordinary skill in the art that the grids must be insulated from each other at the point where they

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cross as recited in claim 7 and it would have been obvious to provide a second material at the point where the grids cross and supporting one of the grids in view of the teaching in figure 7 of Stopper of insulating cross-overs between padlines and netlines (col. 4, lines 20-29). The rejection of claim 7 is sustained.

Claim 8 recites a "semiconductor wafer including a test arrangement for testing a plurality of semiconductor chips" in the preamble. The "test arrangement" is the arrangement of structure in the body of claim 8, which would have been obvious over Stopper for the reasons discussed supra. Claim 8 recites that the intended use of the structure is "so that each of said semiconductor chips can be simultaneously supplied with a test signal." The structure of the power grid in Stopper is manifestly capable of allowing this intended use. We observe that no test signal is positively recited. In any case, however, the term "test signal" is broad enough to include the voltage applied to the power grid in Stopper. Appellant argues that the testing structure can be used after a "static" burn-in or to apply clock pulses during a "dynamic" burn-in (Brief, page 10). However, the "test signal" in claim

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8 is not limited to any specific kind of signal and the voltage applied to the power grid in Stopper is broadly a test signal. Accordingly, the rejection of claim 8 is sustained.

Claim 11 recites that the power supply bus means and the ground bus means are "predominantly formed" of metal film. It would have been obvious to make the power grid of Stopper from a metal film in view of Stopper's teaching that the signal runs are made from a one micron layer of aluminum (col. 13, lines 3-9 and 51-56) because power bus lines need to be made from a material with good conductivity, such as aluminum. It is not clear that "predominantly formed of metal film" requires other material. "Predominate" means "to hold advantage in numbers or quantity." Webster's New Collegiate Dictionary (1977). The term "predominantly" appears broad enough to encompass bus means that are wholly formed of metal film. Claim 11 does not require the specific low electrical resistance portions recited in claim 10. The rejection of claim 11 is sustained.

Claim 12 recites a "method of testing a plurality of semiconductor chips while they are still on a single wafer" in the preamble. The "forming" steps of claim 12 form structure

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which would have been obvious over Stopper for the reasons discussed supra. Claim 12 recites "simultaneously supplying each of said semiconductor chips with a test signal through said power supply bus means." Claim 12 positively recites a test signal but does not define the nature of such signal. The "test signal" is not limited to any specific kind of signal and the voltage applied to the power grid in Stopper is broadly a test signal. The rejection of claim 12 is sustained.

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Claims 2-5, 9, and 10

Claims 2 and 9 require fuse means interposed between one of the power supply bus means and the ground bus means and one of the chips. The examiner relies on Quinn to show a fuse (Examiner's Answer, page 4). Quinn discloses that redundant or optional circuits can be connected or disconnected by blowing fuses by a laser or electrically using additional contacts (col. 6, lines 48-64). While it is true that the fuses in Quinn can be burned out electrically by an excess current, Quinn does not disclose disposing fuses between the power supply bus and a chip or between the ground bus and a chip. The examiner states that the "claims are directed to a semiconductor structure no matter how actually made, therefore the manner by which the chips have been isolated does not distinguish over the prior art" (Examiner's Answer, page 5). However, the claims recite a specific location for the fuse which is not addressed. In our opinion, the examiner has failed to establish a prima facie case of obviousness because the rejection does not address the location of the fuse elements recited in claims 2 and 9. The rejection of claims 2

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and 9 is reversed, as is the rejection of claim 3 which depends on claim 2.

Claim 4 recites that the bus line includes low resistance portions of a material different from the material of the bus lines which facilitates cutting the wafer into blocks which each include a semiconductor chip. This refers to the low resistance wiring lines 8 in appellant's figures 1 and 4. The only place where the examiner's rejection addresses the limitations of claims 4 and 10 appears to be the statement that "bus line structures in both Stopper et al. and Quinn et al. can be and are cleanly cut" (Examiner's Answer, page 7). This ignores the limitations of low resistance portions being formed of a material different from the material of the bus lines (claim 8). Neither Stopper nor Quinn disclose that the bus lines can be formed of separate portions and, therefore, the examiner has failed to establish a prima facie case of obviousness with respect to claim 4. The rejection of claim 4 and claim 5, which depends on claim 4, is reversed.

Claim 10 does not clearly require the "portions" to be of a different material than the bus lines, but does recite that portions be "formed of a low electrical resistance material,

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which can be cut cleanly." The specification describes that aluminum is not cut cleanly by a dicing blade, but tends to have metal whiskers (substitute specification, pages 9-10). Therefore, the aluminum power grid in Stopper and, for example, the aluminum contact pad 6-05 in the "street" in figure 6 of Quinn do not meet the limitations of claim 10. The examiner's statement that "bus line structures in both Stopper et al. and Quinn et al. can be and are cleanly cut" (Examiner's Answer, page 7) provides no reasoning to counter the statement in the specification that aluminum lines are not cleanly cut. The examiner has failed to establish a prima facie case of obviousness with respect to claim 10. The rejection of claim 10 is reversed.

#### CONCLUSION

The rejection of claims 1, 6-8, 11, and 12 is sustained.

The rejection of claims 2-5, 9, and 10 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

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| LEE E. BARRETT              | ) |                 |
| Administrative Patent Judge | ) |                 |
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|                             | ) | BOARD OF PATENT |
| JAMESON LEE                 | ) | APPEALS         |
| Administrative Patent Judge | ) | AND             |
|                             | ) | INTERFERENCES   |
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| RICHARD TORCZON             | ) |                 |
| Administrative Patent Judge | ) |                 |

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