THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 14

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JEAN-PAUL MIFSUD, and
STUART RAPOPORT

Appeal No. 96-1983
Application 08/222,784[1]

ON BRIEF

Before JERRY SMITH, FLEMING, and TORCZON, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-9, which

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[1] Application for patent filed April 04,1994.

constitute all the claims in the application. An amendment after final rejection was filed on May 08, 1995 but was denied entry by the examiner [Paper no. 10].

The invention pertains to a circuit which identifies defective redundant word lines in a Static Random Access Memory (SRAM) macro provided with an Array Built-In Self-Test (ABIST) unit and a redundant mechanism. Specifically, the structure detects failures in a manner which permits a two-pass fuse blow process. The second fuse blow can be performed either in a manufacturing environment, before or after burn-in, or in a system environment should electrical fuses be available.

Representative claim 1 is reproduced as follows:

1. A circuit for allowing a two-pass fuse blow to an integrated circuit of a memory type comprising:

i) memory means having a plurality of word lines, said memory including:

a standard array,

a redundant array provided with redundant word lines,

a decoder means coupled to said standard array, and

comparator means coupled to said redundant array and to said decoder means;

the circuit further comprising:

ii) ABIST means driving said memory means for providing said memory means with self-test patterns;

iii) data compression means responsive to said ABIST means and to said memory means for detecting and [sic] address of at least one of said word lines in said memory means that is defective; and

iv) fail register means responsive to said ABIST means and to said data compression means for storing an address of a defective word line and for generating a number indicative of the number of defective word lines that exceeds the number of redundant word lines of said redundant array,

v) said comparator means for comparing the addresses of said word lines with the addresses of said defective word lines and for selecting a predetermined word line of said redundant array;

vi) OR-gate means having inputs for receiving signals generated by said comparator means and having an output connected to a latching means; and

vii) AND-gate means having a first input connected to said latching means and a second input responsive to signals generated by said data compression means, for generating a signal at an output thereat which is indicative of a defective line of said redundant word lines.

The examiner relies on no references.

Claims 1-9 stand rejected under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly claim the invention.

Rather than repeat the arguments of appellants or the

examiner, we make reference to the brief and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the arguments in support of the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the brief along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that claims 1-9 particularly point out the invention in a manner which complies with 35 U.S.C. § 112. Accordingly, we reverse.

With respect to independent claim 1, the examiner's objections are directed to a lack of clear antecedent basis [line 4, "said memory"], a typographical error [line 14, "and apparatus"], several objections that functional language of the claim is indefinite and lacks proper structural support, and whether the "latching means" [line 29] is part of the

circuit. In the final rejection, the examiner simply included the other claims in the rejection as having similar errors to claim 1 and as depending from claim 1. In the answer, however, the examiner has specifically identified some of these “similar” errors in claims 2, 4 and 5 for the first time. The specific errors noted in claims 2, 4 and 5 were not designated as a new ground of rejection, and appellants have not responded to the examiner’s specific objections with respect to dependent claims 2, 4 and 5.

Appellants have specifically responded to each of the objections raised by the examiner with respect to claim 1. In general, appellants argue that the scope of the invention as recited in claim 1, and as recited in all claims, would be perfectly clear to the person having ordinary skill in the art and the examiner’s rejection is completely unwarranted [brief, pages 6-12].

The general rule is that a claim must set out and circumscribe a particular area with a reasonable degree of precision and particularity when read in light of the disclosure as it would be by the artisan. In re Moore, 439 F.2d 1232, 1235, 169 USPQ 236, 238 (CCPA 1971). Acceptability

of the claim language depends on whether one of ordinary skill in the art would understand what is claimed in light of the specification. Seattle Box Co., v. Industrial Crating & Packing, Inc., 731 F.2d 818, 826, 221 USPQ 568, 574 (Fed. Cir. 1984).

We are unable to find merit in any of the examiner's objections to claim 1. First, the phrase "said memory" in line
4 of claim 1 cannot possibly be misinterpreted because there is only one memory or memory means recited in the claim. Second, typographical errors are not properly the subject of a rejection under 35 U.S.C. § 112. The examiner can always correct typographical errors at the time of allowance. Third, the examiner's objections regarding the functional language and the structural connections do not make any sense. Independent claim 1 clearly recites how the various components (means) are interconnected, and the recitation of the components as "means" allows the components to be claimed according to the functions which are performed. Therefore, we do not understand what the examiner finds unclear and indefinite about the structural and functional recitations of

claim 1. Finally, the examiner's objection as to where the "latching means" [line 29] is located does not properly raise a question of indefiniteness. The OR-gate means of claim 1 is connected to "a latching means." The location of this latching means is not relevant to the question of definiteness. The location of the latching means relates to the breadth of the claim and to nothing else.

We agree with appellants that the artisan having considered the specification of this application would have no difficulty ascertaining the scope of the invention recited in independent claim 1. Since the examiner had indicated in the final rejection that the objections to dependent claims 2-9 were of the same type as discussed for independent claim 1, we also find that the scope of these claims would be clear to the artisan having considered the specification of this application. We do note for the record, however, that the examiner's technical objection of claim 4 in the answer is correct. That is, the phrase "said OR-gate" in line 5 should be --said 3-way OR-gate-- to distinguish the 3-way OR-gate of claim 4 from the OR-gate of claim 1. We see no reason why this technical error cannot be corrected by examiner's

amendment at the time of allowance. In summary, the rejection of claims 1-9 under the second paragraph of 35 U.S.C. § 112 is not sustained. Therefore, the decision of the examiner rejecting claims 1-9 is reversed.

REVERSED

Jerry Smith Administrative Patent Judge	)
Michael R. Fleming Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
Richard Torczon Administrative Patent Judge	)

dm

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