

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KOSHI SETO and YUKIMASA UEMURA

Appeal No. 96-3200
Application No. 08/337,196¹

HEARD: July 15, 1999

Before KRASS, FLEMING, and BARRY, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed November 7, 1994. According to appellants, this application is a continuation of Application No. 07/925,661, filed August 7, 1992, now abandoned.

This is a decision on appeal from the final rejection of claims 12 through 22, all the claims remaining in the application.

The invention pertains to microprocessors. More particularly, a microprocessor simultaneously processes data corresponding to a plurality of computer programs such that the microprocessor switches programs from one to another each time one of the instructions is processed. One of the programs is being processed at all times. A plurality of data each representing an order in which program counters are selected is stored. An optimal program counter selection order can be momentarily determined on the basis of the data stored.

Representative independent claim 12 is reproduced as follows:

12. A microprocessor for processing data corresponding to a plurality of computer programs, comprising:

a plurality of program counters, each one of said plurality of program counters specifying a program address of one of said plurality of computer programs having data to be currently processed by said microprocessor;

means for storing information indicating a plurality of orders in which each of said plurality of program counters is to be selected;

means for sequentially selecting each of said plurality of program counters in accordance with said information stored in said storing means;

an arithmetic logic unit for sequentially processing data of computer programs corresponding to program addresses stored in said program counters sequentially selected by said selecting means; and

means for transferring data between said plurality of program counters, said selecting means, and said arithmetic logic unit, wherein a user can designate said order in which each of said plurality of program counters is to be selected by said selecting means by writing said information indicating said order into said storing means.

The examiner relies on the following references:

Watson et al. (Watson) 1971	3,573,852	Apr. 6,
Lee et al (Lee) 1994	5,367,678	Nov. 22,

(filed Dec. 6, 1990)

Claims 12 through 22 stand rejected under 35 U.S.C. 103 as unpatentable over Watson in view of Lee.

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

OPINION

We reverse.

With regard to the independent claims, the examiner contends that Watson taught a plurality of program counters

(column 18, lines 25-49), means for selecting one of the program counters (column 19, line 35-column 20, line 28), an ALU (400), means for transferring (column 2, lines 1-14; Figure 13) and means for storing the information indicating the order (431n, 431m). The examiner admits that Watson lacks an express teaching for storing a plurality of orders, although it is contended that Watson does teach a register in which the ordering of the schedule is alterable by the ALU and the allocation of the time interval is determined by the code set in the register. The examiner then relies on Lee for a teaching of a plurality of schedules available for various tasks and combines this teaching with Watson, stating that it would have been obvious "to modify the teaching of Watson...with that of Lee...because it would improve the efficiency of the system by allowing for predetermined optimization of the schedule for given task [sic]" [answer-page 5].

The instant claimed invention calls for a single microprocessor to simultaneously process a plurality of programs. Watson, on the other hand, discloses a plurality of processors which share an ALU. A sequence control 418 in

Watson specifies a plurality of virtual processors in sequence of use. However, as argued by appellants [brief-page 6], in Watson, "not a plurality of sequences, as in the case of the present invention, but only one sequence is stored..."

Now, it may be, as apparently contended by the examiner, that the peripheral processor 11 of Watson may be considered to be the single microprocessor, as claimed, and the plurality of virtual processors, which form a part of the peripheral processor, may be considered to be the claimed "program counters," since Watson explains, at column 18, lines 25-27, that the virtual processors comprise program counters. One might even make the argument that these program counters are "selected," as claimed, because, at column 19, lines 34-37, Watson explains that the time available to one or more of the virtual processors may be allocated.

But, even assuming all this to be true and applicable to the instant claims, claims 12 and 22 each require, inter alia, in one form or another, that one may designate the order in which each of the program counters is to be selected by the selecting means. Claim 12 specifically recites "wherein a user can designate said order..." [emphasis ours]. Clearly, there

is nothing in any of the applied references suggesting that a user may designate an order in which the program counters are to be selected and for this reason, alone, we would reverse the rejection of claim 12, and of claims 13 through 21 dependent thereon, under 35 U.S.C. 103.

We find nothing in Watson suggestive of a processing unit selecting one of a number of orders in which program counters are selected. In Watson, the system determines the order in which the virtual processors use the ALU. That order appears to be limited to a single order. There is no predetermined plurality of orders as in the instant claimed invention. The examiner is aware of this and turns to Lee.

While the examiner relies on Lee for a teaching of a predetermined plurality of schedules available for various tasks, we agree with appellants that Lee "assigns a single task to a number of processors, an operation quite distinct from that of the present invention" [brief-page 7]. Thus, a single task of a single program is executed by using a plurality of processors in Lee. As observed by appellants, the schedulers of Lee "cannot momentarily change the order in which a number of programs are executed..." [brief-page 8]. Thus, we do not

see any teaching within Lee that remedies the deficiency of Watson with regard to a predetermined plurality of orders wherein a user can designate the order in which each of a plurality of program counters is to be selected by a selecting means.

Lee does disclose, at column 5, lines 12-17,

In one embodiment of the present invention, a plurality of schedules are available for various sets of tasks implemented by a plurality of processors. Each time the processors receive their programs, a transaction schedule associated with the particular set of programs is loaded into the controller.

Accordingly, it would appear that Lee does indicate some kind of a "plurality of orders," each of which may be selected, dependent upon a set of tasks to be implemented. However, since Lee is short on details as to how the "plurality of schedules" is implemented, other than to say that a "transaction schedule associated with the particular set of programs is loaded into the controller," it would appear speculative to make the determination that Lee does, indeed, suggest the instant claimed

means for sequentially selecting each of said plurality of program counters, said selecting means having a plurality of independent storing means for storing information indicating a plurality of orders

in which each of said plurality of program counters is to be selected.

In any event, counsel for appellants indicated at the oral hearing on July 15, 1999 that since the instant claims are in "means plus function" language, 35 U.S.C. 112, paragraph 6, requires us to look to the instant disclosure for the disclosed means and equivalents thereof which the claim language is intended to cover. We agree, and so we find that the instant claim language relating to "means for sequentially selecting..." is limited to the structure depicted in instant Figure 1B and "equivalents thereof." We do not find any such structure in either Watson or Lee that is equivalent to, or even similar to, that which is shown in instant Figure 1B. Accordingly, we find that the combination of Watson and Lee would not have made the narrowly construed subject matter of claims 12 through 22 obvious, within the meaning of 35 U.S.C. 103.

Accordingly, the examiner's decision rejecting claims 12 through 22 under 35 U.S.C. 103 is reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
MICHAEL R. FLEMING)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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