

**THIS OPINION WAS NOT WRITTEN FOR PUBLICATION**

The opinion in support of the decision being entered today  
(1) was not written for publication in a law journal and  
(2) is not binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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***Ex parte*** ROBERT S. GRONDALSKI

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Appeal No. 96-4088  
Application 08/317,411<sup>1</sup>

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ON BRIEF

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<sup>1</sup> Application for patent filed October 3, 1994. According to Appellant, the application is a continuation of Application 07/826,907, filed January 24, 1992, abandoned; which is a continuation-in-part of Application 07/121,563, filed November 16, 1987, now U.S. Patent No. 5,230,079, issued July 20, 1993; which is a continuation-in-part of Application 06/909,013, filed September 18, 1986, now U.S. Patent No. 4,985,832, issued January 15, 1991; and a continuation-in-part of Application 07/018,937, filed February 25, 1987, abandoned.

Appeal No. 96-4088  
Application 08/317,411

Before BARRETT, FLEMING and GROSS, *Administrative Patent Judges*.

FLEMING, *Administrative Patent Judge*.

**DECISION ON APPEAL**

This is a decision on appeal from the final rejection of claims 1 through 8, all the claims pending in the present application.

The invention relates to array processing systems which incorporate a large number of processors that are interconnected in a regular connection structure and in which all processors receive the same instruction from a common control structure. In particular, the invention relates to a processing array where each of the processing elements includes a parity generating circuit for generating a parity bit for an outgoing message transmitted to another processing element, and it also includes a parity check circuit for checking parity of an incoming message that is received by that processing element. The parity checking and parity generating circuits are separate from each other and enable the process-

ing element to generate parity for one message while simultaneously checking parity of the other message.

Independent claim 1 is reproduced as follows:

1. A processing array comprising:

a plurality of processing elements; and

a bidirectional interconnection network disposed to directly connect all of adjacent neighboring processing elements for each of said plurality of processing elements for carrying data messages between any of the adjacent neighboring processing elements,

wherein each of said processing elements of said plurality of processing elements comprises:

a parity generating circuit for generating a parity bit for a first data message that is transmitted by that processing element over the interconnection network to another processing element among said plurality of processing elements; and

a parity checking circuit for checking parity of a second data message as it is received by that processing element over the interconnection network, said parity checking and parity generating circuits being separate from each other and enabling that processing element to generate parity for the first data message being sent by that processing element while simultaneously checking parity of the second message being received by that processing element.

The Examiner relies on the following references:

Sze	4,346,474	Aug. 24, 1982
Chin et al. (Chin)	4,823,347	Apr. 18, 1989

Appeal No. 96-4088  
Application 08/317,411

Claims 1 through 8 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sze in view of Chin.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the brief and answer for the respective details thereof.

**OPINION**

We will not sustain the rejection of claims 1 through 8 under 35 U.S.C. § 103.

The Examiner has failed to set forth a *prima facie* case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. *In re Sernaker*, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be

Appeal No. 96-4088  
Application 08/317,411

considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied***, 117 S.Ct. 80 (1996) ***citing W. L. Gore & Assoc., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

On page 6 of the brief, Appellant argues that the Examiner has not shown how the references, whether taken alone or in combination, describe or suggest "a processing array comprising . . . a bidirectional interconnection network disposed to directly connect all of adjacent neighboring processing elements . . . for carrying data messages between any of the adjacent neighboring processing elements . . . and enabling that processing element to generate parity for the first data message being sent by that processing element while simultaneously checking parity of the second message being received by that processing element" as recited, for example, in Appellant's independent claim 1. Similarly, Appellant argues on page 13 that neither Sze nor Chin describes or

Appeal No. 96-4088  
Application 08/317,411

suggests "an output data path disposed to directly connect to all of adjacent neighboring processing elements . . . a parity checking circuit connected to the input data path, said parity checking circuit checking parity of the second data message as said second data message is received over the input path and while the first data message is being sent out over the output data path" as recited in Appellant's claim 8.

Appellant further emphasizes on pages 7 through 9 of the brief that not all of the recited steps are described or suggested by the combination of Sze and Chin.

Upon a close review of both Sze and Chin, we agree that not all the claim elements are described or suggested by the combination of Sze and Chin. In particular, we note that Sze teaches an even-odd parity checking for synchronous data transmission. In column 3, lines 5-30, Sze discloses that Figure 1 illustrates a representative communications system in which the present inventive improvement may be used. In particular, Sze discloses three data receiving and transmission

Appeal No. 96-4088  
Application 08/317,411

stations 1, 2 and 3 coupled to each other in a loop. Station 1 can transmit data to station 2. Station 2 can transmit data to station 3 and station 3 can transmit data back to station 1. Thus, Sze fails to disclose Appellant's claimed bidirectional interconnection network disposed to directly connect all the adjacent neighboring processing elements for each of the plurality of processing elements for carrying data messages between any of the adjacent processing elements in a processing array. In column 4, lines 35-67, Chin discloses a data transmission between a pair of data interchange units 12 and 14 which exchange the data on a high-speed, bidirectional data bus 16 extended across the interface. However, Chin fails to disclose a processing array comprising a plurality of processing elements and a bidirectional interconnection network disposed to directly connect all of the adjacent neighboring processing elements for each of the plurality of processing for carrying out data messages between any of the adjacent neighboring processing elements as recited in Appellant's claim 1.

Appeal No. 96-4088  
Application 08/317,411

Neither reference teaches enabling a processing element to generate parity for a first data message being sent for that processing element while simultaneously checking parity of a second message being received by that processing element as recited in Appellant's claim 1. Upon a review of Sze, we find that Sze fails to teach enabling a processing element to generate parity for a first data message while simultaneously checking parity of a second message. Furthermore, we fail to find that Chin teaches this element as well. We agree with the Examiner that Chin teaches two sets of control signals being transferred in opposite directions across a data transmission interface in a first data transfer period, during which their joint parity is determined and latched on each side of the interface, and the results of one latched joint parity termination is transmitted across the interface. However, we fail to find Chin's teaching of enabling a processing element to generate parity for a data message while simultaneously checking parity of a second data message. In

Appeal No. 96-4088  
Application 08/317,411

column 2, lines 29-67, Chin clearly discloses that their invention is not concerned with data transmission but is concerned with the use of parity signals to validate the transmission of control signals across an I/O limited, high-speed, bidirectional data transmission interface. Chin is not concerned about using parity in the normal data transmission in normal operation.

Appellant argues on pages 9 and 10 of the brief that there is no basis to combine Sze and Chin. Appellant, in particular, argues that Chin teaches that it is important to provide error checking over control signals transferred between a pair of data interface units, but Chin is not attempting to perform data parity checking and furthermore teaches away from bidirectional error checking. Appellant argues that it is difficult to understand the Examiner's contention that someone skilled in the art would be motivated to combine a system for isolating malfunctioning units by means of a single unidirectional error checking signal path with Sze's serial loop parity checking system.

Appeal No. 96-4088  
Application 08/317,411

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

We find no reason to combine Chin with Sze to obtain the Appellant's claimed invention. Sze is concerned with providing parity checking for a synchronous data transmission in a unidirectional serial loop transmission system. Chin is concerned not with providing parity checking for data transmission but instead is using parity checking to determine if control signals are being transferred properly. We fail to find any reason to modify Chin to provide a parity checking for data transmission, nor do we find any motivation to modify Sze to become an array processing system with bidirectional data transmission. Therefore, we will not sustain the

Appeal No. 96-4088  
Application 08/317,411

Examiner's rejection of claims 1 through 8 under 35 U.S.C. §  
103 as being unpatentable over Sze in view of Chin.

We have not sustained the rejection of claims 1  
through 8 under 35 U.S.C. § 103. Accordingly, the Examiner's  
decision is reversed.

**REVERSED**

	LEE E. BARRETT	)	
	Administrative Patent Judge	)	
		)	
		)	
		)	BOARD OF
PATENT		)	
	MICHAEL R. FLEMING	)	APPEALS AND
	Administrative Patent Judge	)	
INTERFERENCES		)	
		)	
		)	
	ANITA PELLMAN GROSS	)	
	Administrative Patent Judge	)	

MRF:psb  
Patent Law Group  
Digital Equipment Corporation  
111 Powdermill Road  
MS02-3/G3  
Maynard, MA 01754-1499