

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No.39

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte BRENT A. FAIRBANKS

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Appeal No. 1996-4089  
Application 08/227,293<sup>1</sup>

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ON BRIEF

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Before KRASS, BARRETT, and FRAHM, Administrative Patent Judges.

FRAHM, Administrative Patent Judge.

DECISION ON APPEAL

Appellant has appealed to the Board from the examiners' final rejection of claims 17, 18, and 20 to 26, which constitute all of the pending claims in the application before us on appeal. Claims 1 to 16 and 19 have been canceled.

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<sup>1</sup> Application for patent filed April 13, 1994. According to appellant, the application is a continuation of Application 07/968,593, filed October 29, 1992, now abandoned.

## BACKGROUND

The subject matter on appeal is directed to a method for checking logic design rules in a computer-aided logic design system prior to physical implementation of the logic circuit. (See specification, page 1; Brief, page 3). More specifically, the method involves comparing an initial logic design file with a design rule and notifying a user of any rule violations. (See specification, page 1; Brief, page 3). As indicated in the Brief (pages 4 to 8), appellant's recited logic design verification method applies specific design rules in an effort to check a design and warn a user in the event of an unsatisfactory design. In general, appellant's invention recited in claims 17, 18, 20, and 26 on appeal provides for four specific design rules: (1) "to check whether more than one clock signal generation means is used in the logic design" (claims 17 and 26); (2) to check "if more than two gates are present between the clock signal input of a component and the clock signal generation means" (claims 18 and 26); (3) to "determine[] permitted and prohibited clear signal distribution schemes" (claims 20 to 25 and 26); and (4) to check "if a synchronous device that is synchronized to a first clock signal receives data that is synchronized to a second clock signal" (claim 26). As further discussed, infra, we find that the applied references fail to teach or suggest at least specific design rules (1) through (3) as these salient limitations are recited in claims 17, 18, and 20 to 26 on appeal.

Representative method claim 17 is reproduced below:

17. A method executing in a computer-aided logic design system for designing and testing logic circuitry prior to physical implementation, wherein the method verifies compliance of a logic design with

a preselected set of design rules that specify logical relationships between electrical signals, wherein the logic design includes one or more electrical signals, wherein the logic design includes clock signal generation means for outputting a clock signal, wherein the clock signal generation means is coupled to one or more components having a clock signal input, the method comprising the following steps:

providing a design rule to check whether more than one clock signal generation means is used in the logic design;

providing a logic design file incorporating the initial logic design in computer-readable form;

comparing at least portions of the initial design to the design rule; and

providing a user-discernable indication of any violation of the design rule by the initial logic design.

The following references are relied on by the examiners:

Binoeder et al. (Binoeder)	4,620,302	Oct. 28, 1986
Omoda et al. (Omoda)	4,899,273	Feb. 6, 1990
Yoshida	5,105,374	Apr. 14, 1992
Watkins et al. (Watkins)	5,220,512	Jun. 15, 1993 (effectively filed Apr. 19, 1990)
Lipton	5,220,662	Jun. 15, 1993 (filed Mar. 28, 1991)

Varma, Prab (Varma), "TDRC - A Symbolic Simulation Based Design For Testability Rules Checker," 1990 International Test Conference, Paper 46.1, pages 1055-64.

Claims 17 and 18 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiners rely upon Watkins in view of Varma.

Claims 20 to 25 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the

examiners rely upon Watkins in view of Lipton, Yoshida, Omoda, or Binoeder.

Claim 26 stands rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiners rely upon Watkins in view of Varma and Lipton.

Rather than repeat the positions of appellant and the examiners, reference is made to the Brief and the Answer for the respective details thereof.

#### OPINION

For the reasons generally set forth by appellant in the Brief, and for the reasons which follow, we will reverse the rejection of claims 17, 18, and 20 to 26 under 35 U.S.C. § 103. As a consequence of our review, we are in agreement with appellant that the claims on appeal would neither have been taught nor suggested by the references of record (see Brief, pages 9 to 16 and 26 to 27).

In reaching our conclusion on the issues raised in this appeal, we have carefully considered appellant's specification and claims, the applied patents, and the respective viewpoints of appellant and the examiners. As a consequence of our review, we are in general agreement with appellant that the applied references would neither have taught nor suggested the methods of designing and testing logic circuitry of appellant's claims on appeal. For the reasons which follow, we will reverse the decisions of the examiners rejecting claims 17, 18, and 20 to 26 under 35 U.S.C. § 103.

Appellant argues (Brief, pages 9 to 11 and 26 to 27) that Watkins and Varma fail to teach or suggest the specific design rules as recited in claims 17, 18, and 26 (rules (1) and (2) as discussed

supra). We agree, and we find that the features of checking whether more than one clock signal generation means is used in the logic design (claims 17 and 26), and of checking if more than two gates are present between the clock signal input of a component and the clock signal generation means (claims 18 and 26), are neither taught nor would have been suggested by the applied prior art. We agree with appellant (Brief, pages 9 to 10) that Varma, at the pages cited by the examiners (see Varma, pages 1055, 1056, 1058, and 1059), fails to teach or suggest the specific rules (e.g., rules (1) and (2)) of claims 17, 18, and 26 on appeal. We cannot agree with the examiners (Answer, pages 9 to 11) that one of ordinary skill in the art looking at Watkins, and specifically Varma, would have been motivated to check the specific design rules recited in the claims of checking whether more than one clock signal generation means is used and of checking if more than two gates are present between the clock signal input of a component and the clock signal generation means based on the very general rationale of "identify[ing] real problems in a real ASIC designs" (Varma, page 1063). Accordingly, we cannot sustain the rejection of claims 17, 18, and 26 under 35 U.S.C. § 103.

We are also in agreement with appellant (Brief, pages 11 to 16) that Watkins and Lipton fail to teach or suggest the specific design rule recited in claims 20 to 26 (rule (3) as discussed supra). We find that the specific feature of determining permitted and prohibited clear signal distribution schemes (claims 20 to 25 and 26) is neither taught nor would have been suggested by the applied prior art. We cannot agree with the examiners (Answer, pages 5 to 6 and 12 to 15) that one or any of the applied

secondary references to Lipton, Yoshida, Omoda, or Binoeder would have taught or suggested the specific design rule (rule (3)) of determining permitted and prohibited clear signal distribution schemes. The examiners admit that Watkins fails to teach providing this specific design rule (Answer, page 5), and then rely on any of Lipton, Yoshida, Omoda, or Binoeder to teach this feature. However, the examiners notably fail (Answer, pages 5 to 6) to assert that any of the secondary references specifically teach determining permitted and prohibited clear signal distribution schemes (claims 20 and 26), or any of the other specific rules (see claims 21 to 25), and instead aver that these rules are "well known methodologies" that would have been obvious to implement in order to optimize circuit operation. Accordingly, we cannot sustain the rejection of claims 20 to 26 under 35 U.S.C. § 103.

With respect to claims 20 to 26, we further note our agreement with appellant (Brief, pages 11 to 12) that Watkins and Lipton teach away from each other since Watkins (as well as appellant's claims 20 to 26) concerns circuit design and testing which takes place prior to physical circuit implementation, whereas Lipton pertains to testing done after physical circuit implementation.

Although we find that the examiners have made a prima facie case of obviousness as to the appealed claims, we conclude that appellant has rebutted this prima facie case by successfully showing that the specific design rules of the appealed claims are neither taught nor would have been fairly suggested by the secondary references. In view of the foregoing, the decisions of the examiners rejecting claims 17, 18, and 20 to 26 under 35 U.S.C. § 103 are reversed.

Appeal No. 1996-4089  
Application 08/227,293

CONCLUSION

The decision of the examiners rejecting claims 17 and 18 under 35 U.S.C. § 103 over Watkins in view of Varma is reversed.

The decision of the examiners rejecting claims 20 to 25 under 35 U.S.C. § 103 over Watkins in view of Lipton, Yoshida, Omoda, or Binoeder is reversed.

The decision of the examiners rejecting claim 26 under 35 U.S.C. § 103 over Watkins in view of Varma and Lipton is reversed.

REVERSED

ERROL A. KRASS	)	
Administrative Patent Judge	)	
	)	
	)	
	)	
LEE E. BARRETT	)	BOARD OF PATENT
Administrative Patent Judge	)	APPEALS AND
	)	INTERFERENCES
	)	
ERIC FRAHM	)	
Administrative Patent Judge	)	

Appeal No. 1996-4089  
Application 08/227,293

Townsend and Townsend and Crew  
Two Embarcadero Center  
Eighth Floor  
San Francisco, CA 94111