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The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RAUL A. GARIBAY, JR.
and
MARC A. QUATTROMANI

Appeal No. 1997-0300
Application 08/138,790

ON BRIEF

Before HAIRSTON, JERRY SMITH and FLEMING, **Administrative
Patent Judges.**

FLEMING, **Administrative Patent Judge.**

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 11 through 24. Claims 1 through 10 have been canceled.

The invention, as described by Appellants on page 6 of the specification,¹ relates to a microprocessor which has a write buffer located between the core of a microprocessor and a memory. Appellants identify on pages 11 and 59 of the specification, that the memory receives data over a 64 bit data bus (eight bytes). On page 19 of the specification, Appellants identify that the function of the write buffer is to receive data from the core. This data is to be written to memory. Appellants identify on page 21 of the specification that the buffer entries contain the data and the physical memory address where the data is to be stored. The buffered information is then later written to memory when the memory is not busy with higher priority operations. Thus, the core more rapidly performs memory write functions. On pages 59

¹ The page numbers referenced throughout this opinion correspond to those of the originally filed specification, and not the substitute specification filed on March 22, 1995.

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through 63 of the specification, Appellants describe how the write buffer is used in performing misaligned writes.

Appellants describe a misaligned write on page 59 of the specification as a write where the data written to memory will overlap the memory's eight byte boundary for a particular memory address.

Accordingly, a second write is needed for the additional information. Appellants identify on pages 59 and 60 of the specification that there is a control logic which determines if the write operation will exceed the eight byte boundary. If the operation will exceed the eight byte boundary, a second entry to the write buffer will be made and this second entry will be loaded with the address for the memory location where the data which carries over the eight byte boundary is to be written.

Independent claim 11 is illustrative of the invention.

11. A microprocessor having a data path of predetermined length that defines a memory block boundary, comprising:

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(a) core means for executing a plurality of write instructions to produce a plurality of write operands, each write operand including a data field and an address field;

(b) misalignment control means, coupled to the core means, for indicating if any of the address fields of the plurality of write operands are misaligned with respect to the memory block boundary;

(c) write buffer means having a plurality of entries, coupled to the core means and the misalignment control means, for temporarily storing the plurality of write operands and responsive to the misalignment control means indicating a misaligned write operand, for allocating a first and a second write buffer entry, wherein the address field of the first write buffer entry contains a beginning address in a first memory block for the misaligned write operand and the address field of the second write buffer entry contains a continuation address in a second memory block for the misaligned write operand; and

(d) memory means having a plurality of data field entries, coupled to the write buffer means, for storing the data fields of the plurality of write operands.

The Examiner relies upon the following references:

Shimp et al (Shimp)	3,916,388	Oct. 28, 1975
Ardini Jr. et al. (Ardini)	4,959,771	Sept. 25, 1990

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Claims 11 through 24² stand rejected under 35 U.S.C. § 103 as being unpatentable over Shimp and Ardini.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the briefs³ and the answer for the respective details thereof.

OPINION

We will not sustain the rejections of claims 11 through 24 under 35 U.S.C. § 103.

The Examiner has not set forth a *prima facie* case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed

² It is noted that the Examiner and Appellants are in disagreement as to whether Claims 11 and 16 contain the word "length" or "width." As there are no rejections or amendments addressing this language on the record, there is no issue before us concerning this claim language. Accordingly, this opinion addresses the claims as submitted by Appellants in the January 10, 1996 appeal brief as appendix A. Nonetheless, our decision concerning the rejection on appeal does not rely upon an interpretation of the disputed claim language.

³ Appellants filed an appeal brief on January 10, 1996. Appellants filed a reply brief on May 20, 1996. On November 1, 1996, the Examiner mailed a communication stating that the reply brief has been entered and considered.

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invention by the express teachings or suggestions found in the prior art or by the implication contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied***, 519 U.S. 822 (1996) (***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984)).

Appellants argue on page 8 of the appeal brief (brief) that Shimp and Ardini combined do not teach the claimed invention. Specifically, Appellants argue on pages 5 and 6 of the brief that Shimp teaches away from the invention as Shimp does not teach a write buffer between the core and the memory. On page 6 of the brief, Appellants also assert that though Ardini teaches a write buffer, the write buffer is used in conjunction with "unaligned writes." Appellants assert that

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"unaligned" writes are "completely different from 'misaligned' writes and therefore there is no incentive to look to Shimp." Further, Appellants point out that Ardini does not address a write across a 64 bit word boundary as Appellants claim.

On page 2 of the Examiner's answer (answer), the Examiner asserts that the combination of Shimp and Ardini teach the claimed write buffer as "the two write accesses generated by Shimp et al.'s system will cause Ardini Jr. et al.'s system to allocate two write buffer entries, with each containing the address of that memory word to which the data in that buffer entry is destined." On page 3 of the answer, the Examiner asserts that Ardini provides the motivation of enhanced performance by buffering of memory writes.

First, we must determine the scope of the claims. We find that the scope of the independent claims includes a microprocessor which writes data to memory through a write buffer which temporarily stores the data. Further, the scope includes that when there is a misalignment between the data and the memory

block boundary, the write buffer has two entries, the first containing the beginning address in memory for the data storage and the second being the memory address for the continuing data. These limitations are found in the claim 11, a "core means for executing a plurality of write instructions," and a

write buffer means having a plurality of entries, coupled to the core means and the misalignment control means, for

temporarily storing the plurality of write operands and responsive to the misalignment control means indicating a misaligned write operand, for allocating a first and a second write buffer entry, wherein the address field of the first write buffer entry contains a beginning address in a first memory block for the misaligned write operand and the address field of the second write buffer entry contains a continuation address in a second memory block for the misaligned operand.

Claim 16 contains similar limitations of a "core for executing . . ." and "a write buffer . . ." Claim 21 contains similar limitations of " a core . . . a write buffer" and the step of "allocating a first and a second write buffer entry . . ." In summary, we find that the scope of the independent claims is such that if a write from the core to

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memory will cross the memory block boundary, the write buffer will have two entries, the first entry having the address of the memory location where the beginning of the data is to be stored

and the second entry having the address of the continuing memory location.

Turning to the rejection based upon 35 U.S.C. § 103, we find that Shimp teaches a microprocessor system where the data output by the processor can be of fewer bytes than the number of bytes of data that can be stored in one memory location. See column 1, lines 34 to 39. To avoid wasting memory by allocating

a small number of bytes of data to a multi-byte memory location, the data is stored in contiguously packed multi-byte units which are not equal to memory word width. See column 1, lines 39 to 45. As a result, the data from the processor may cross memory boundaries which requires two writes to store the data in two memory locations. See column 7, lines 55 to 59.

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We find that Ardini teaches a microprocessor system where data to be written to memory is sent from the processor to a write buffer (buffer) for temporary storage in the buffer. See column 5, lines 45 through 54. Ardini teaches that the micro-processor writes data as either 16 or 32 bits and that both the write buffer and memory can accept 64 bits of data. See column 4, lines 1 through 5 and 22 through 25. We find that Ardini teaches making a determination of whether the data written to the buffer is to be stored in successive memory locations. If so, the data is merged together and stored in memory with one write from the write buffer (i.e. data from the microprocessor, which contains fewer bytes than the width of the memory are merged with other data into one write to one memory location). See column 1, lines 51 through 66, and column 5, lines 13 through 44. We find that Ardini teaches that the timesaving advantage of the buffer is that it reduces the number of writes

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to memory by merging the writes together, i.e. for a 64 bit bus, two 32 bit writes will be merged into one 64 bit write. See column 1, lines 51 through 66, and column 4, lines 38 through 52. Thus, we find that these features of Ardini teach that data should be grouped into one write where possible. Further, we fail to find that Ardini teaches or suggests use of the buffer to make writes across memory boundaries. Rather, we find that the purpose of Ardini is to make the largest write within the memory's boundaries.

We fail to find that Ardini provides motivation to modify Shimp in the manner asserted by the Examiner. Our reviewing court has stated that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n. 14 (Fed. Cir. 1992) (***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)). We find that Shimp's system makes two writes to different memory addresses. See column 7, line 58.

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This is illustrated in Table XII and Table XIII in columns 17 and 18. We find that Table XII shows that the first write enters bytes A through D in one physical memory location, and the second write

stores bytes E through G in the second location. As stated above, we find that Ardini teaches that using the buffer allows writes to contiguous memory locations to be merged into one write to one memory location. Thus, Ardini's system, when presented with the writes shown in Shimp's Table XII, would not make a misaligned write. Rather, the data would be written as one seven bit write to one memory location. Thus, we find that Ardini does not suggest the desirability to add a write buffer to Shimp's system which writes across memory boundary. Accordingly, we will not sustain the rejection under 35 U.S.C. § 103 as being unpatentable over Shimp and Ardini.

For the foregoing reasons, we reverse the rejection of claims 11 to 24 under 35 U.S.C. § 103.

REVERSED

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