

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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***Ex parte*** DOUGLAS D. GEPHARDT and KELLY M. HORTON

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Appeal No. 1997-0416  
Application No. 08/125,406

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ON BRIEF

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Before JERRY SMITH, LALL, and DIXON, **Administrative Patent Judges**.  
DIXON, **Administrative Patent Judge**.

**DECISION ON APPEAL**

This is a decision on appeal from the examiner's final rejection of claims 1-20, which are all of the claims pending in this application.

We REVERSE.

## **BACKGROUND**

The appellants' invention relates to a system and method for restarting a peripheral bus clock signal and requesting mastership of a peripheral bus. The stopping and restarting of the clock are disclosed as a power saving feature. An understanding of the invention can be derived from a reading of exemplary claim 14, which is reproduced below.

14. A method for re-starting a peripheral bus clock signal and requesting mastership of a peripheral bus comprising the steps of:

stopping said peripheral bus clock signal upon the occurrence of a predetermined condition;

generating an asynchronous clock request signal within an alternate bus master;

re-starting said peripheral bus clock signal in response to said asynchronous clock request signal; and

generating a synchronous bus request signal within said alternate bus master to request mastership of said peripheral bus after said peripheral bus clock signal has been re-started, wherein said synchronous bus request signal is synchronous to said peripheral bus clock signal.

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The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Herrig et al. (Herrig)	4,835,737	May 30, 1989
Murphy	5,128,970	Jul. 07, 1992
Smith et al. (Smith)	5,167,024	Nov. 24, 1992

Admitted prior art in Figure 1

Claims 1-4, 7-8 and 14-18 stand rejected under 35 U.S.C. § 103 as being unpatentable over Admitted prior art in Figure 1 in view of Herrig and Murphy. Claims 5, 6, 9-13<sup>1</sup> and 19-20 stand rejected under 35 U.S.C. § 103 as being unpatentable over Admitted prior art in Figure 1, Herrig and Murphy in view of Smith.

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellants regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 11, mailed Sep. 4, 1996) for the examiner's reasoning in support of the rejections, and to the amended appellants' brief (Paper No. 14, filed Dec. 5, 1997) for the appellants' arguments thereagainst.

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<sup>1</sup> We note that the examiner has rejected claims 12 and 13 in the body of the rejection, but did not include these 2 claims in the heading.

## **OPINION**

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by the appellants and the examiner. As a consequence of our review, we make the determinations which follow.

Appellants argue that there should be four separate groupings of claims paralleling the chain of claim dependency. Appellants have not provided separate argument beyond arguing claims 1 and 9. Therefore, we will address only two groupings which correspond to the groupings in the examiner's rejections. We will address claims 14 and 9 which are the broadest claims in each respective group.

### **CLAIMS 1-4, 7-8 AND 14-18**

Appellants argue that none of the prior art applied against the claims addresses the problem of power saving with peripheral clocks when using alternative bus masters as disclosed on pages 2-3 of the specification. (See brief at pages 5-7.) We agree with appellants. Appellants argue the limitations of claim 1 and that the prior art does not meet these recited functions. (See brief at pages 9-10.) We agree with appellants. Claim 14 is broader than the argued limitations of claim 1 and we will address the language of claim 14 as it relates to these arguments.

While claim 14 is directed broadly to a method of stopping and starting a peripheral bus clock, the language of claim 14 requires that the alternate bus master must generate “an asynchronous clock request signal within an alternate bus master” and the peripheral bus clock must be restarted “in response to said asynchronous clock request signal” and then “generating a synchronous bus request signal within said alternate bus master to request mastership of said peripheral bus after said peripheral bus clock signal has been re-started, wherein said synchronous bus request signal is synchronous to said peripheral bus clock signal.” The examiner combines various teachings in the rejection and concludes that the combined teachings would meet the claimed invention, but the examiner has not provided a convincing line of reasoning to achieve the claimed invention. While each of the incremental steps of the process may have been generally known, the examiner has not addressed the problem set forth in the specification with respect to presence of alternative bus masters in a system and the need for a synchronous bus request therefrom. In the discussion of the admitted prior art, the specification specifies that if the peripheral bus clock is not operational then the bus request cannot be performed in the prior art Figure 1. With the proposed combination of Herrig with respect to halting the bus clock and restarting of the bus clock after physical manipulation of a board, there would not be a signal requesting restart of the clock as required by claim 14. Moreover, we find no motivation in Herrig for having an alternative bus master request a clock restart.

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Furthermore, we find that the examiner has not provided a line of reasoning thereto, and the examiner has not cited any portion of Herrig besides Figure 1, items 112 and 120-127. The examiner maintains that the restart of the clock is “in response to [an] assertion of a signal indicating bus clock is again needed.” (See answer at page 4.) The examiner has not addressed that the bus master is requesting the restart of the clock rather than an actuation of a switch.

With respect to the examiner's response to the appellants' arguments, the examiner generally maintains that appellants are arguing the references individually and does not address the merits of these arguments. (See answer at page 9-11.) The examiner strings numerous case citations together, but does not apply these recited citations to the combination of teachings. Therefore, the examiner's responses are not persuasive.

Appellants argue that the examiner has used impermissible hindsight to reconstruct the claimed invention. (See brief at pages 8-9.) We agree with appellants. The examiner has attempted to find the parts of the claimed invention and reconstruct the claimed invention, and we find the examiner has not provided a convincing line of reasoning to modify the prior art teaching to meet the claimed invention. Therefore, we cannot sustain the rejection of claim 14. Similarly, we cannot sustain the rejection of independent claims 1 and 18 which contain similar limitations.

**CLAIMS 5, 6, 9-13, 19 AND 20.**

With respect to claim 9, Appellants argue that Smith does not remedy the deficiency in the above combination. (See brief at pages 10-11.) We agree with appellants. Again, the examiner is brief in his discussion of and citations to the applied prior art teachings of Smith. (See answer at page 6.) From our review of Smith, Smith is concerned with power management which is controlled by the CPU 12 and power manager (PMGR) 11. We find no disclosure in Smith which teaches or suggests that the peripherals request that the peripheral bus clock be restarted. Smith generally discloses three modes of operation of the computer 10 and monitoring by the PMGR. (See Smith at columns 7 and 8.) Smith discloses that the PMGR monitors lines 37 such that any input from the I/O controller will wake the computer from the sleep state. (See Smith at column 8, lines 21-23.) Clearly, Smith does not disclose the I/O transmitting a request to wake the computer, but rather that the computer monitors to determine when to stop and restart power or clocks within the system using switches 26 and clock control 27 to wake and resume operation. Therefore, Smith does not remedy the deficiency in the combination of the admitted prior art, Herrig and Murphy. Hence, we cannot sustain the rejection of claim 9 and dependent claims 5, 6, 10-13, 19 and 20.

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**CONCLUSION**

To summarize, the decision of the examiner to reject claims 1-20 under 35 U.S.C. §  
103 is reversed.

REVERSED

JERRY SMITH	)	
Administrative Patent Judge	)	
	)	
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	)	
	)	BOARD OF PATENT
PARSHOTAM S. LALL	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
	)	
	)	
	)	
JOSEPH L. DIXON	)	
Administrative Patent Judge	)	

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APPLICATION NO. 08/125,406

APJ DIXON

APJ JERRY SMITH

APJ LALL

DECISION: **REVERSED**

Prepared By: Leticia Pihulic

**DRAFT TYPED:** 24 Jan 01

**FINAL TYPED:**