

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today  
(1) was not written for publication in a law journal and  
(2) is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte SYDNEY W. POLAND

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Appeal No. 1997-0918  
Application 08/160,301<sup>1</sup>

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ON BRIEF

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Before THOMAS, JERRY SMITH and BARRETT, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellant has appealed to the Board from the examiner's  
final rejection of claims 1 through 8 and 32 through 36.

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<sup>1</sup> Application for patent filed November 30, 1993.

Representative claim 1 is reproduced below:

1. A method for performing division in a data processing apparatus comprising the steps of:

storing a divisor in a first data register;

storing a numerator in a second data register;

storing a status bit in a status register;

selecting an intermediate data word as either data stored in said second data register or data stored in a third data register based upon said status bit stored in said status register;

left shifting said intermediate data word one bit position;

storing said left shifted intermediate data word in said second data register thereby replacing data previously stored in said second data register;

subtracting said divisor stored in said first data register from said left shifted intermediate data word thereby forming a difference;

storing said difference of said left shifted intermediate data word and said divisor in said third data register thereby replacing data previously stored in said third data register;

determining whether said difference is less than zero;

setting said status bit stored in said status register based upon whether said difference is less than zero; and

setting a quotient bit based upon whether said difference is less than zero.

The following references are relied on by the examiner:



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said first data register from said left shifted intermediate data word thereby forming a difference." The focus of the argument is that Yamaoka fails to teach subtracting a divisor from the left shifted intermediate data word. Appellant continually asserts that this reference operates in such a manner that the left shifted intermediate data word is the output of the shifter 2 which is fed to register A0 and not to the adder/subtractor 1 of Figure 3 of Yamaoka. In the brief and the various reply briefs appellant argues that Yamaoka clearly shows that it is the unrotated output of selector 6 that is supplied to the X input of the adder/subtractor 1 of Figure 3 of this reference. Appellant indicates that the output of the shifter 2 is stored in register A0 and is not supplied to the input of this adder/subtractor circuit 1 as required by claims 1 and 5 on appeal.

For his part, the examiner correctly argues, in our view, that the claimed feature is recited and taught in the reference as argued by the examiner in the responsive arguments portion of the answer at the top of page 8 thereof. This position is maintained in the succeeding answers.

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For our purposes, we make general reference to the teachings shown in Figure 3 of Yamaoka and the corresponding discussion at column 3, lines 34 through line 68, the discussion beginning at topic (d) at column 4, line 63 through the end of column 5 and, most succinctly, the statements made in a summary manner at column 6, line 38 through 52.

Thus, it is apparent that in the next succeeding operation, it may occur that the output of register A0 (previously shifted in shifter 2 before being stored therein) is operated upon after having been selected by the selector 6 in a subtraction operation performed by the adder/subtractor 1 of Yamaoka. The bottom of page 4 at least of appellant's initial reply brief indicates in the table that the output of selector 6 is the intermediate data word for purposes of the claims. This is consistent with the arguments presented at page 5 of the initial brief. However, in contrast to subsequent arguments made in subsequent reply briefs, appellant asserts in a supplemental reply brief of July 19, 1996, that the operation, as just pointed out by the examiner, is considered by appellant to be a conditional step where the

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selection is not conditional according to the claimed version in claims 1 and 5 on appeal. In our view, the examiner correctly points out at the bottom of page 1 of the supplemental examiner's answer filed on July 31, 1996 that the version of claims 1 and 5 has no unconditional recitation to justify appellant's argument. In fact, this is somewhat an anomalous argument because the title of appellant's invention indicates that there is a conditional source selection of a prior difference or a left shifted remainder according to the invention anyway. Note also page 243, lines 8 and 9 of appellant's disclosure.

In any event, it is clear from the teachings of Yamaoka that under certain conditions, the selector 6 does select the previously determined intermediate data word, which has been previously left shifted by shifter 2 and placed in register A0 and then is fed by line 6A to the adder/subtractor 1 in accordance with the subtraction feature argued in accordance with the recitations of both independent claims 1 and 5 on appeal.

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In view of the foregoing, and in view of appellant's grouping of the claims at page 4 of the principal brief on appeal, and due to the fact that there are no arguments presented as to the further specifics of independent claim 5 and dependent claims 2 through 4 and 6 through 8, all these claims fall with appellant's arguments restricted to the feature common to both independent claims 1 and 5 on appeal just discussed.

Before we address the features recited in dependent claims 32 and 35 as argued by appellant at pages 6 and 7 of the principal brief on appeal, we observe that appellant has not argued any substantive distinction with respect to Zaidi used by the examiner in combination with Yamaoka nor has appellant argued that the references were not properly combined within 35 U.S.C. § 103.

As to the feature common to dependent claims 32 and 35, appellant argues only the showings and features taught and suggested in Yamaoka and not those provided by Zaidi. In the discussion bridging pages 6 and 7 of the principle brief,

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appellant points out that Yamaoka fails to disclose any relationship for the most significant bit of the intermediate data word to any structure employed for determining a difference less than zero. In other words, appellant is only arguing the features in the second clause or recitation of dependent claims 32 and 35 relating to the "logical OR" operation being dependent upon a carry out signal and the most significant bit of said intermediate data word.

It is clear from the abstract of Zaidi, the summary of the invention at column 2, the showings in Figures 3 and 4, the discussion in the paragraph bridging columns 5 and 6, as well as the discussion of Figures 3 and 4 at columns 7 and 8 of Zaidi, that a logical ORing-type of operation is performed by the XNOR circuit 20 in Figure 3 and it is based upon a carry out signal from the ALU 12 and the MSB bits in accordance with the features recited in independent claims 32 and 35 on appeal.

Turning next to the recitation of the common features recited in claims 33 and 36, appellant indicates at page 7 of

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the principal brief on appeal that these claims require that the same source, namely, a result of the logical OR operation controls both the source selection for the subtraction operation and the generation of the quotient bit. On the other hand, we recognize as did appellant argue that Yamaoka fails to show this. Appellant notes that Figure 3 of Yamaoka shows the operative carry detector 4 controlling the selection of the selector 6, which has already been previously argued by appellant to be functionally equivalent to the status bit operation. The relationship of this to a logical OR operation has been previously established by our analysis with respect to claims 32 and 35. Again, we make reference to the earlier noted portions of Zaidi which indicate that the output of the XNOR circuit 20 serves as a quotient bit indication as recited at the end of dependent claims 33 and 36 on appeal.

Finally, we turn our attention to the subject matter of dependent claim 34 on appeal which is argued by appellant at page 8 of the principal brief on appeal. As noted by appellant there, the examiner has apparently made no attempt to correlate the features of Yamaoka and Zaidi to the features

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of claim 34, which is similar to the recitation in dependent claims 33 and 35 in part. Claim 34 recites that the arithmetic logic unit has a carry input to it, a feature which is not taught or suggested or shown in either Yamaoka's Figure 3 or Zaidi's Figure 3. Therefore, we reverse the rejection of this claim.

In view of the foregoing, we have sustained the rejection of claims 1 through 8, 32, 33, 35 and 36, but have reversed the rejection of dependent claim 34. Accordingly, the decision of the examiner is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

James D. Thomas )  
Administrative Patent Judge )  
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PATENT	Jerry Smith	) BOARD OF
	Administrative Patent Judge	) APPEALS AND
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