

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHARLES K. ERDELYI
and JOHN E. GERSBACH

Appeal No. 97-0951
Application 08/148,452¹

ON BRIEF

Before THOMAS, BARRETT, and LALL, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed November 8, 1993, entitled "Slew Rate Control Circuit."

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This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-24.

We reverse.

BACKGROUND

The disclosed invention is directed to a slew rate control circuit for controlling current turn-on or turn-off rates, i.e., the "slew rates," and a voltage regulator for providing dual reference voltages to the slew rate control circuit.

Claim 1 is reproduced below.

1. A slew rate control circuit comprising:

a pair of inverter circuits;

each of said inverter circuits comprising first and second transistors and being coupled between current limiting transistors;

an output current switch comprising a pair of switching transistors, each pair of said switching transistors being coupled through a respective node to a respective one of said inverter circuits; and

means, including a current regulator circuit, for providing a set of current levels in the inverter circuits to define the current available for charging and discharging the capacitance on each respective node.

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The examiner relies on the following prior art:

Banura	4,972,136	November 20, 1990
Wong et al. (Wong)	4,987,324	January 22, 1991
Yamate et al. (Yamate)	5,182,497	January 26, 1993
Brewer	5,237,209	August 17, 1993

The teachings of the references are fairly described in Appellants' Brief.

Claims 1, 3, and 14 stand rejected under 35 U.S.C. § 103 as being unpatentable over Wong and Banura.

Claims 4, 15, and 17-24 stand rejected under 35 U.S.C. § 103 as being unpatentable over Wong, Banura, and Brewer.

Claims 2, 5-13, and 16 stand rejected under 35 U.S.C. § 103 as being unpatentable over Wong, Banura, Brewer, and Yamate.

We refer to the Final Rejection (Paper No. 7, misnumbered as Paper No. 6 in the file) (pages referred to as "FR__") and the Examiner's Answer (Paper No. 16) (pages referred to as "EA__") for a statement of the Examiner's position and to the Appeal Brief (Paper No. 13) (pages referred to as "Br__") for a statement of Appellants' arguments thereagainst.

OPINION

Claim language

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There appear to be some minor problems with the claim language which has not been addressed by the Examiner. In claims 1 and 14, in "each pair of said switching transistors being coupled through a respective node to a respective one of said inverter circuits," the word "pair" should be deleted. In claim 3, the first and second current source transistors appear to refer to the same elements as the first and second transistors in claim 1; if not, it is not clear what the first and second transistors in claim 1 refer to.

Claims 1, 3, and 14

We have trouble understanding the Examiner's rejection because the Examiner merely states that "Wong discloses the claimed device except for a current limiting transistor, a current regulator circuit and the use of bi-polar transistors" (FR3) and does not provide an element-by-element comparison between the claim elements and the elements in Wong. The way the claims are intended to be read on Wong is not clear. Claims 1 and 14 are directed to the slew rate control circuit of figures 2 and 3. We

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compare Appellants' figure 2 with figure 4 in Wong. The claimed "pair of inverter circuits" corresponds to elements 58 and 59 in Appellants' figure 2. Presumably, the Examiner reads the "pair of inverter circuits" on inverters A and B in Wong because a capacitance must be charged and discharged through the inverter and the only capacitance shown in Wong is at the output node V_0 . Under this interpretation, we do not find "an output current switch comprising a pair of switching transistors" corresponding to DAC current switch 49 with switching transistors 53 and 55 in Appellants' figure 2.

If the Examiner reads the "pair of inverter circuits" on inverters C and D in Wong and the "output current switch comprising a pair of switching transistors" on the inverter B having a pair of transistors Q1B and Q2B, then we find that the circuit fails to operate to charge and discharge a capacitance on the node between inverter C and transistor Q1B or on the node between inverter D and transistor Q2B; no capacitance is shown at these nodes. If the Examiner is relying on some other interpretation of the claims, it should be expressly stated.

Thus, we have a fundamental problem with the rejection because it finds that Wong teaches more than it appears to. However, assuming, arguendo, that Wong did teach everything except for the limitations of "said inverter circuits . . . coupled between current limiting transistors" (e.g., the inverter 58 in figure 2 is coupled between current limiting transistors 75 and 77) and "means, including a current regulator circuit, for providing a set of current levels in the inverter circuits . . .," we find no motivation in Banura to modify Wong to provide these features.² The inverters in Wong are connected directly between the supply voltage V_{DD} and ground and the output is connected to the output V_o ; thus, Wong has a fixed current flow through the inverters. There is no disclosure or suggestion in Wong to use serially arranged current limiting transistors as claimed.

Banura discloses a linear power regulator with a MOSFET 80 arranged for connection between an input voltage source V_i and a load. A difference amplifier 85 maintains a

² Since we do not find bipolar transistors recited anywhere in claims 1, 3, or 14 we do not understand why the Examiner states that Wong does not teach this feature.

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fixed ratio between a reference voltage at Zener diode 70 and the output voltage V_o . Current limiting circuitry 24 senses the current that the power supply provides to the load and disables the MOSFET 80 when the current exceed a predetermined value. Appellants' sketches of the circuits of the invention, Wong, and Banura (Br13) fairly show the differences between the circuits. Banura discloses a current limiting transistor 80, but since Banura is not directed to controlling the current through an inverter or to controlling the current for charging and discharging the capacitance on a node in a slew rate control environment, we must agree with Appellants' arguments (Br14) that there is no indication why or how these two circuits could be combined.

The Examiner has not indicated how the references could possibly be combined. The Examiner concludes that "[i]t would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the invention of Wong with a current limiting transistor and a current regulator circuit of Banura, in order to provide an efficiency, that includes a low loss current limiter with a

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very sharp cutoff and high temperature stability . . ."

(FR3). This does not explain why one skilled in the art would have sought to apply the current limiting transistor for a linear voltage regulator in Banura to the slew rate control circuit of Wong or how the references would be combined. While it is true that the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference, this does not mean that finding isolated features is all that is needed to establish obviousness. There must be some explanation how the teachings of the references are proposed to be combined to produce the claimed invention. The Examiner has failed to establish a prima facie case of obviousness. The rejection of claims 1, 3, and 14 is reversed.

Claims 4, 15, and 17-24

Claim 4 depends on claim 3 which depends on claim 1 and additionally recites a regulator circuit. Independent claims 15 and 19 are directed to the regulator circuit itself.

The Examiner states (FR3-4):

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Wong discloses applicant's claimed invention but does not disclose the usage of a second voltage output, voltage clamping means and a regulated voltage source. A second voltage output mainly depends upon the requirements of the circuit, if the a [sic] second output is necessary to the function of the circuit then it should be included, if not then it is not included. It would have been obvious at the time of [sic] invention was made, to a person having ordinary skill in the art to [?] a slew rate controller as disclosed by Wong and Banura, and combine it with the use of a second voltage output, provides [sic] several output voltages at different and varied ranges was known to be reasonably pertinent to [the] art of Wong.

This rejection does not address any of the limitations of the regulator circuit except, perhaps, the general use of a second voltage output. Since the Examiner correctly finds that Wong does not disclose a regulator circuit, it would seem that the rejection should address the limitations of "first, second, and third current conducting legs" with the limitations of what elements are contained in each leg. However, it does not. The rejection does not even mention the added patent to Brewer. Brewer is directed to a charge pump circuit for providing bipolar voltage outputs. The Examiner makes no attempt to correlate the teachings of Brewer with the limitations of the claims at issue. It appears that the Examiner has used Brewer simply for its teaching of two outputs, which fails to even marginally

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address the claim limitations. We agree with Appellants' argument that the configuration of the claimed regulator circuit is not taught or hinted at by Wong, Banura, or Brewer. The Examiner has failed to establish a prima facie case of obviousness. The rejection of claims 4, 15, and 17-24 is reversed.

Claims 2, 5-13, and 16

Claim 2 depends on claim 1 and recites a voltage clamping means coupled to the nodes. Independent claim 5 is similar to claim 14, but recites a voltage clamping circuit coupled to the nodes between the inverters and a control circuit.

The Examiner finds that Yamate discloses a clamping circuit and concludes that it would have been obvious to add the clamping circuit of Yamate to the slew rate controller of Wong, as modified by Banura and Brewer. It is noted that Brewer has not been applied to claim 1; however, since claim 1 does not have the regulator circuit limitation that Brewer (apparently) was cited for, we treat this as a harmless error.

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As discussed in connection with the rejection of claim 1, it is not known how the Examiner is applying Wong. In particular, we do not know which inverters in Wong the Examiner considers to be the claimed inverters and which elements the Examiner considers to be the pair of switching transistors. Under either of the interpretations we presented, we find no motivation to add a clamping circuit as shown in Yamate. Further, we find no motivation to add current limiting transistors as recited in claims 1 and 5. As discussed in connection with the rejection of claim 15, we find no discussion in the Examiner's rejection of the limitations of the regulator circuit and, thus, we find no motivation to add a regulated voltage source as recited in claim 16. For all these reasons, the Examiner has failed to establish a prima facie case of obviousness. The rejection of claims 2, 5-13, and 16 is reversed.

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CONCLUSION

The rejections of claims 1-24 are reversed.

REVERSED

	JAMES D. THOMAS)	
	Administrative	Patent Judge)
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)	BOARD OF
PATENT			
	LEE E. BARRETT)	APPEALS
	Administrative Patent Judge)	AND
)	INTERFERENCES
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