

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 25

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TIMOTHY J. DELL, GEORGE CHENG-CWO FENG
and MARK W. KELLOGG

Appeal No. 1997-1755
Application 08/163,447

ON BRIEF

Before THOMAS, KRASS and LALL, Administrative Patent Judges.
LALL, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of all the pending claims, 1 and 4 through 8. Claims 2 and 3 have been canceled.

The disclosed invention relates to a semiconductor assembly for providing a plurality of clock-responsive semiconductor devices, most specifically synchronous memory devices, in a packaging arrangement such that the timing of both the data in and data out of the package provides the highest level of confidence of accuracy with respect to time. For semiconductor devices providing a common function on a single package, it is important that common signals reach the individual devices as close to simultaneously as possible. The invention achieves this objective of providing minimal distortion of clock input signals to each of a plurality of memory modules by incorporating a resistor (fixed impedance) connected, as an example, between the package assembly side of connector 15 and the memory module 12 on the semiconductor package 10 (figure 8A).

Claim 1 is reproduced below as illustrative of the invention.

1. A semiconductor assembly comprising:

a plurality of semiconductor devices each responsive to a clocking signal applied to the device via at least one clock input lead associated with said device;

a packaging assembly for supporting said plurality of

Appeal No. 1997-1755
Application 08/163,447

semiconductor devices, each of said semiconductor devices being spaced a predetermined distance from each other;

a plurality of packaging assembly input/output pins arranged in spaced relationship for coupling signals to at least some of said semiconductor devices from an external source;

at least one clock input pin arranged with said input/output pins for coupling a clocking signal to said semiconductor devices;

common clock distribution means coupled between said clock input pin and said clock input leads of said semiconductor devices; and

fixed impedance means connected between said common clock distribution means and a reference voltage, said impedance means being physically located adjacent to said clock input pin and between said clock input pin and said semiconductor devices.

The references¹ relied on by the Examiner are:

Lee et al. (Lee)	4,639,615	Jan. 27, 1987
Lin et al. (Lin)	5,216,278	Jun. 1, 1993

Admitted Prior Art

Irwin, David, "Basic Engineering Circuit Analysis", pages 332-333 (Irwin).

¹ Even though Webster (the dictionary) and Irwin (the circuit analysis book) do not appear in the statement of the final rejection, the body of the final rejection and the Appellants' brief discuss these references. Therefore, we treat them as a part of the final rejection for this appeal.

Appeal No. 1997-1755
Application 08/163,447

"Webster's II", New Riverside University Dictionary, page 978.
(Webster).

Claims 1 and 4 to 8 stand rejected under 35 U.S.C. § 103
over Lee, Lin, Webster, Irwin and the admitted prior art.

Reference is made to Appellants' brief² and the Examiner's
answer for their respective positions.

OPINION

We have considered the record before us, and we will
reverse the rejection of claims 1 and 4 to 8.

With respect to claims 1 and 4 to 8, the Examiner has
failed to set forth a prima facie case of obviousness. It is
the burden of the Examiner to establish why one having
ordinary skill in the art would have been led to the claimed
invention by the express teachings or suggestions found in the
art, or by implications contained in such teachings or

² There are three papers, nos. 12, 18 and 23, marked as a
brief. Paper nos. 18 and 23 are the same, and they differ
from paper no. 12 only in the correction of the formalities.
Since the Examiner addressed paper no. 12 in his answer, and
since there is no difference on merits in later briefs, we
will refer to paper no. 12 as the brief for appeal purposes.

Appeal No. 1997-1755
Application 08/163,447

suggestions. In re Sernaker, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." Para-Ordnance Mfg. v. SGS Importer Int'l, Inc., 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), cert. denied, 117 S.Ct. 80 (1996) citing W. L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

We first take claim 1. After discussing individually the applied references [answer, pages 3 to 4], the Examiner asserts that "one would have been motivated to locate the resistor between the common clock and the reference voltage as taught in Lee et al. in combination with Lin et al. to enhance the clock distribution ..., since it has been held that rearranging parts of an invention involves only routine skill in the art" [id. 4]. Appellants argue that Lee does not teach the application of any "trimmable", or other, elements to a single clock signal to modify the skew of a series of clock signals applied to a single input terminal, and the addition of the teachings of Lin, admitted prior art, Irwin and Webster

Appeal No. 1997-1755
Application 08/163,447

does not cure this fundamental deficiency of Lee [brief, pages 4 to 5]. Appellants also dismiss the Examiner's assertion that the claimed invention merely involves the "rearranging of parts" shown by the applied references [brief, pages 5 to 6]. We agree with Appellants. Whereas, the claimed invention differs from the admitted prior art only in the incorporation of a "fixed impedance means ..., said impedance means being physically located adjacent to said clock input pin and between said clock input pin and said semiconductor devices" (Claim 1), none of the references applied by the Examiner in the final rejection, taken singly or in combination, supplies this feature. Lee is directed to adjusting the output signals of a semiconductor device so that all the output signals are of the same form. A variable impedance is used to adjust the skew rate of the signals to achieve the same form. A fixed impedance would not achieve the result Lee is designed for. Lin too adds nothing to meet the above claimed feature. The mere presence of a resistor in a semiconductor assembly in Lin does not teach the placement of such a resistor in a specific claimed manner. Likewise, Irwin and/or Webster also fail to disclose the above claimed feature. Thus, we conclude that

Appeal No. 1997-1755
Application 08/163,447

the Examiner failed to establish a prima facie case. We do not sustain the obviousness rejection of claim 1 and its dependent claims 4 to 8 over admitted prior art, Lee, Lin, Webster and Irwin.

DECISION

The decision of the Examiner rejecting claims 1 and 4 to 8 under 35 U.S.C. § 103 is reversed.

REVERSED

Appeal No. 1997-1755
Application 08/163,447

	JAMES D. THOMAS)	
	Administrative Patent Judge)	
)	
)	
)	
	ERROL A. KRASS)	BOARD OF
PATENT	Administrative Patent Judge)	APPEALS AND
)	INTERFERENCES
)	
)	
	PARSHOTAM S. LALL)	
	Administrative Patent Judge)	

psl/ki

Appeal No. 1997-1755
Application 08/163,447

Howard J. Walter, Jr.
IBM Corporation
Dept. 915, Bldg. 972-2
1000 River Street
Essex Junction, VT 05452