

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 33

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FERNANDO MACIAS-GARZA,
TODD W. MILLER,
and
MONTGOMERY C. MCGRAW

Appeal No. 1997-2399
Application No. 08/355,104

ON BRIEF

Before THOMAS, HAIRSTON, and HECKER, Administrative Patent
Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims
1 through 28.

The disclosed invention relates to a method and apparatus
for detecting inconsistencies in two microprocessors via the

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use

of arbitration between the two microprocessors for control of a system bus.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. An apparatus for detecting inconsistencies in microprocessors in a computer system having a system bus and memory coupled to the system bus, wherein the memory includes program instructions, the apparatus comprising:

a first microprocessor coupled to the system bus for executing the instructions in the memory when said first processor has control of the system bus;

a second microprocessor coupled to the system bus for executing the instructions in the memory performed by said first processor when said second processor has control of the system bus;

processor control logic coupled to said first processor and said second processor, said processor control logic arbitrating control of the system bus between said first processor and said second processor;

wherein said processor control logic removes said first processor from control of the system bus when said first processor begins a write cycle and grants control of the system bus to said second processor;

wherein said processor control logic returns control of the system bus from said second processor to said first processor when said second processor begins said write cycle, said first processor resuming execution of the instructions in the memory; and

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error detection logic coupled to said first and second processors which compares address and data information generated by each of said processors on said write cycle when said processor control logic returns control of the system bus to said first processor, said logic generating a signal indicative of a match between said address and data signals of said first and second processors.

The references relied on by the examiner are:

Ossfeldt 1978	4,099,241	Jul. 4,
Burrage et al. (Burrage) 20, 1986	4,590,549	May
Williams 1989	4,816,990	Mar. 28,
Cutts, Jr. et al. (Cutts) 1990	4,965,717	Oct. 23,
Kimura 1992	5,136,595	Aug. 4,
		(filed May 24,
1989)		
Best 18, 1992	5,140,680	Aug.
		(filed Apr. 13,
1988)		

Claims 1 through 7, 11, 13, 15 through 20, 23 and 26 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kimura.

Claims 8, 9 and 22 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kimura in view of Williams.

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Claims 10 and 21 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kimura in view of Ossfeldt.

Claims 12 and 24 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kimura in view of Burrage.

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Claims 14 and 25 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kimura in view of Cutts.

Claims 27 and 28 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kimura in view of Best.

Reference is made to the brief and the answer for the respective positions of the appellants and the examiner.

OPINION

The obviousness rejections of claims 1 through 28 is reversed.

Kimura discloses a microprocessor system (Figure 1) that uses a functionally redundant mode (FRM) to check for errors in the operation of two microprocessors. One of the microprocessors operates in a normal mode to drive the buses to output an address, fetch instructions via the bus, execute the fetched instructions, and drive the buses to read or write operand data (column 1, lines 23 through 27). In FRM, the other microprocessor operates in synchronism with the normal mode microprocessor, but does not drive the buses (column 1, lines 27 through 30). The FRM microprocessor simultaneously fetches the same instruction and operand data fetched by the normal

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mode microprocessor and executes the instruction (column 1, lines 30 through 33). The FRM microprocessor compares the addresses and data generated therein with the addresses and data generated and outputted onto the buses by the normal mode microprocessor, and outputs a comparison result (column 1, lines 39 through 44). The FRM microprocessor performs the comparison operation at every bus cycle (column 1, line 53 through 55; column 2, line 11 through 19; column 4, lines 1 through 4).

The examiner recognizes (Answer, page 4) that "Kimura does not explicitly disclose [sic] that each of the processors have access to and control of the system bus at different times under control of processor control logic," but nevertheless concludes that "[i]t would have been obvious to one having ordinary skill in the art to realize that the redundancy processor accesses the busses after the transferring of data signals from the normal processor to the memory in order for the redundancy processor to obtain instruction from the memory."

Appellants argue (Brief, pages 6 through 8) that the

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system control unit 7 and the control logic in the microprocessors used by Kimura specifically prevent the two microprocessors from "alternately sharing control of a common bus." According to the appellants (Brief, page 7), the obviousness rejection would require a complete restructuring of the Kimura reference to make it work in the manner proposed by the examiner, and that "manner

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would be entirely contrary to the expressly stated purpose of the structure disclosed in the reference."

We agree with appellants' arguments. Kimura neither teaches nor would have suggested arbitration between two microprocessors for independent control of a system bus. Accordingly, the obviousness rejection of claims 1 through 7, 11, 13, 15 through 20, 23 and 26 is reversed.

The obviousness rejection of claims 8 through 10, 12, 14, 21, 22, 24, 25, 27 and 28 is likewise reversed because the references to Williams, Ossfeldt, Burrage, Cutts and Best do not cure the noted shortcoming in the teachings of Kimura.

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DECISION

The decision of the examiner rejecting claims 1 through
28 under 35 U.S.C. § 103 is reversed.

REVERSED

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JAMES D. THOMAS)	
Administrative Patent Judge)	
)	
)	
)	BOARD OF PATENT
KENNETH W. HAIRSTON))
Administrative Patent Judge)	APPEALS AND
)	
)	INTERFERENCES
)	
STUART N. HECKER)	
Administrative Patent Judge)	

KWH:hh

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