

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PAUL RYAN and DEAN E. RYAN

Appeal No. 1997-2587
Application No. 08/078,864¹

HEARD: September 15, 1999

Before KRASS, MARTIN and GROSS, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on an appeal from the final rejection of claims 4, 8, 9, 11 through 15 and 17 through 26.

The invention is directed to a globally addressable matrix of electronic circuit elements, best illustrated by

¹ Application for patent filed June 21, 1993.

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reference to representative independent claim 4 reproduced as follows:

4. A globally-addressable array of circuit elements for generating a plurality of pixels having distributed intelligence comprising:

addressable logic circuitry at each pixel circuit element location for receiving gray scale data for a respective pixel circuit element; and,

a common bus means interconnecting the addressable logic circuitry at each of said locations for transferring pixel gray scale data to said logic circuitry from a common data processor.

The examiner relies on the following references:

Green	4,908,613	Mar. 13,
1990		
British patent (Crossland)	2 233 469	Jan. 9,
1991		

Claims 4, 8, 9, 25 and 26 stand rejected under 35 U.S.C. § 102(b) as anticipated by Green.

Claims 11 through 15 and 17 through 24 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner cites Green with regard to claims 14, 15, 17 and 21

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through 24, adding Crossland with regard to claims 11 through 13 and 18 through 20.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

We will sustain the rejection of claim 4 under 35 U.S.C. § 102(b) as anticipated by Green and the rejection of claim 21 under 35 U.S.C. § 103 as unpatentable over Green. However, we will not sustain the rejection of any other claim based on the evidence provided by the applied references.

Turning first to claim 4, the examiner indicates that the "addressable logic circuitry at each pixel circuit element location" is met by counter 2 at each pixel in Green. The examiner also indicates that common load data bus means, 3, of Green meets the claimed "common bus means."

Appellants take issue with the examiner's position, arguing that Green does not disclose the claimed addressable logic circuitry or the common bus means. Rather than a common bus that transmits both data and an address so that each pixel's logic circuitry can accept the data directed towards it, Green, as argued by appellants at pages 4-5 of the principal brief, "relies on a specific sequence of data shifted over a common load data bus, and necessarily places the data in a time sequence determined by the location of the pixel, because each pixel location relies upon the previous

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pixel location for an enable signal to latch and retain data which is destined for it."

While we recognize the differences between the instant disclosed invention and that disclosed by Green, we agree with the examiner that independent claims 4 and 21 are of such breadth that the claimed subject matter is anticipated (claim 4) and made obvious (claim 21) by Green.

While appellants argue that there is no addressable logic circuitry at each pixel element in Green which can identify its unique address in a data stream appended to gray scale data for that pixel circuit element, claims 4 and 21 do not require such a "unique" address.

With regard to the logic circuitry, claim 4 requires only that there is "addressable logic circuitry at each pixel circuit element for receiving gray scale data...." Clearly, the counters, 2, of Green may be said to receive gray scale data [see column 2, lines 22-24]. Also, these counters are "addressable," as broadly claimed, in the sense that something is addressing them in order to load the required data. In Green's case, each pixel circuit instructs, or "addresses," an adjacent circuit that it is next to be loaded. Thus, as

broadly set forth in claim 4, we agree with the examiner that Green's counters 2 may be considered "addressable logic circuitry." Even though each pixel element in Green is "addressed," or instructed, in a time sequence determined by the location of the pixel, the data employed by each pixel is still originating from a common data processor and the common bus means, 3, of Green interconnects the "addressable logic circuitry," or counters, 2, at each of the pixel locations for transferring pixel gray scale data to the counters.

Similarly, with claim 21, this claim requires logic circuitry for receiving pixel values representing a gray scale level for an LED² and a means for addressing the logic circuitry. For the reasons, supra, it is our view that Green's counters, 2, do constitute a "logic circuitry," as broadly claimed, and that something does, indeed, "address" these logic circuits.

With regard to claim 21, appellants further argue that the claimed subject matter distinguishes over Green because the means for addressing the logic circuitry is capable of

² Appellants do not take issue with the obviousness of using LEDs, rather than LCDs, as in Green.

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addressing "any one of said logic circuitry...." Again, while we understand the difference between the instant disclosed invention and that disclosed by Green and we understand that the counters of Green are addressed sequentially, it is our view that the instant claimed subject matter is broader than appellants would have us believe. Any time one of the counters is being addressed, or instructed, by an adjacent circuit, it can be said that one of the logic circuitry or "any one of the logic circuitry" is being addressed. The claim does not specify that any one of the circuits is randomly addressed or that any one of the circuits can be addressed at any given time and not in any particular sequence. It recites the addressing of "any one" of the logic circuits and, broadly speaking, whenever a counter in Green is being instructed to load, that particular counter, at that time, is "any one" of the logic circuitry.

Accordingly, we will sustain the rejections of claims 4 and 21.

We will not, however, sustain the rejection of claim 8 [under 35 U.S.C. § 102(b)] or claim 15 [under 35 U.S.C. § 103] because these claims particularly recite that the addressable

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logic circuitry has a "unique" address identifying its location for storing data representing the gray scale of the pixel element. We find no such "unique" address associated with the counters of Green. Since we will not sustain the rejections of claim 8 and claim 15, their dependent claims 9, 11 through 14, 17 through 20, 25 and 26 will stand with claims 8 and 15.

We also will not sustain the rejection of claims 22 through 24 under 35 U.S.C. § 103. Claim 22 makes it clear that the logic circuitry has a pair of conductors interconnecting each pixel element and that one of the conductors is connected to a clock signal line while the other conductor is connected to supply serial pixel address data and serial pixel gray scale data to the logic circuitry. We find no such disclosure or suggestion in Green and the examiner has not particularly indicated what, in Green, is relied on for such a teaching. Claims 23 and 24 stand with claim 22.

We have sustained the rejections of claim 4 [under 35 U.S.C. § 102(b)] and claim 21 [under 35 U.S.C. § 103] but we have not sustained the rejections of claims 8, 9, 25 and 26

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[under 35 U.S.C. § 102(b)] or of claims 11 through 15, 17
through 20 and 22 through 24 [under 35 U.S.C. § 103].

Accordingly, the examiner's decision is affirmed-in-part.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOHN C. MARTIN)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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