

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte YVON BAHOUT and FRANCOIS TAILLIET

Appeal No. 1997-2984
Application No. 08/259,967

ON BRIEF

Before HAIRSTON, BARRY, and LEVY, Administrative Patent Judges.
BARRY, Administrative Patent Judge.

DECISION ON APPEAL

The examiner rejected the appellants' claims 26-28. They appeal therefrom under 35 U.S.C. § 134(a). We reverse.

BACKGROUND

The invention at issue in this appeal relates to computer buses. A computer bus comprises specialized lines. Some lines convey functional signals such as control, address, data, and clock signals. Two of the other lines supply voltage signals. For example, buses that conform to the I2C standard comprise an "SDA" line for the transmission of control, address, and data

signals; an "SCL" line for the transmission of a clock signal; a "Vss" line assigned to a ground potential; and a "Vcc" line for the transmission of a positive supply potential.

The appellants' invention is aimed at reducing the number of lines of an I2C standard bus while preserving compatibility with its communications protocol. The standard bus is translated to a modified bus with an added line, which is complementary to a clock signal of the system. The two power supply lines of the standard bus are eliminated from the modified bus. The supply potentials of these lines are instead regenerated from the clock signal and its complement using a full-wave rectifier.

Claim 26, which is representative for present purposes, follows:

26. A method for reducing the number of lines in a bus system comprising the steps of:

receiving, on a bus input, at least one data signal, a first clock signal, a first system potential, and a second system potential;

producing a second clock signal which is complementary to said first clock signal;

transmitting said data signals and said first and second clock signals over a bus;

(Examiner's Answer at 7.) The appellants argue, "Wilson does not remotely suggest the step of 'producing a second clock signal which is complementary to said first clock signal', nor the step of 'transmitting said data signals and said first and second clock signals over a bus'." (Appeal Br. at 10.)

Claim 26 specifies in pertinent part the following limitations: "receiving, on a bus input, at least one data signal, a first clock signal, a first system potential, and a second system potential; producing a second clock signal which is complementary to said first clock signal; transmitting said data signals and said first and second clock signals over a bus" Accordingly, the limitations require inter alia inputting a data signal and a clock signal, generating a clock signal complementary to the inputted clock signal, and transmitting the inputted clock signal, the complementary clock signal, and the inputted data signal over a bus.

The examiner fails to show a disclosure of the limitations in the applied prior art. "A prior art reference anticipates a claim only if the reference discloses, either expressly or inherently, every limitation of the claim. See Verdegaal Bros.,

Inc. v. Union Oil Co., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "[A]bsence from the reference of any claimed element negates anticipation.'" Rowe v. Dror, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997) (quoting Kloster Speedsteel AB v. Crucible, Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986)).

Here, Wilson describes "[a] power supply circuit for converting a digital signal to a [direct current] DC voltage" Col. 1, ll. 65-66. Although "[a] pair of input lines **20** and **21** [of the reference's power supply circuit] are coupled to receive digital input signals labeled Tx(+) and Tx(-)," col. 2, ll. 8-10, neither of the input signals is a clock signal. To the contrary, both are data signals. Specifically, "[t]he differential signal lines ... carry digital data" Abs., ll. 2-4.

Because neither of the signals inputted to Wilson's power supply circuit is a clock signal, we are not persuaded that the applied prior art discloses the limitations of "receiving, on a bus input, at least one data signal, a first clock signal, a first system potential, and a second system potential; producing

a second clock signal which is complementary to said first clock signal; transmitting said data signals and said first and second clock signals over a bus" Therefore, we reverse the rejection of claim 26 and of claims 27 and 28, which depend therefrom.

CONCLUSION

In summary, the rejection of claims 26-28 under § 102(b) is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
LANCE LEONARD BARRY)	APPEALS
Administrative Patent Judge)	AND
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STUART S. LEVY)	
Administrative Patent Judge)	

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APPEAL NO. 1997-2984 - JUDGE BARRY
APPLICATION NO. 08/259,967

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Prepared By: APJ BARRY

DRAFT SUBMITTED: 06 Jun 03

FINAL TYPED:

Team 3:

I typed all of this opinion.

Please check spelling, cites, and quotes.

Do NOT change matters of form or style.

For any additional reference provided, please prepare PTO 892 and include copy of references