

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte MATHIAS GRUETZNER,  
WILFRED HARTMANN, and CORDT-WILHELM STARKE

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Appeal No. 1997-3129  
Application 08/301,743

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ON BRIEF

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Before BARRETT, FLEMING, and RUGGIERO, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 1-20, all of the claims pending in the present

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application. An amendment after final rejection filed June 13, 1996, was approved for entry by the Examiner.

The claimed invention relates to a test circuit for testing the interconnect wiring between two chips of a plurality of integrated circuit chips. More particularly, Appellants indicate at pages 3 and 4 of the specification that selector circuitry on one of the plurality of chips selects two chips for interconnect testing and enables the transfer of test data between the two chips.

Claim 1 is illustrative of the invention and reads as follows:

1. A multi-chip semiconductor structure capable of providing interconnect testing capability, comprising:

a plurality of integrated circuit chips including a first chip and a second chip;

said first chip having a first transceiver and a first storage coupled to said first transceiver;

said second chip having a second transceiver and a second storage coupled to said second transceiver;

a selector circuit on one of said plurality of chips and coupled to all of said plurality of chips, said selector circuit having a circuit portion capable of controlling selection of said first and said second chip for the interconnect testing, said selector circuit further capable of selectively enabling said first and said second transceiver to enable transfer of test data from said first storage to said second storage.

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The Examiner relies on the following prior art:

Sauerwald et al. (Sauerwald)                      4,791,358                      Dec.  
13, 1988

Claims 1-20 stand finally rejected under 35 U.S.C. § 103  
as being unpatentable over Sauerwald.<sup>1</sup>

Rather than reiterate the arguments of Appellants and the  
Examiner, reference is made to the Briefs<sup>2</sup> and Answer for the  
respective details thereof.

OPINION

We have carefully considered the subject matter on  
appeal, the rejection advanced by the Examiner and the  
evidence of obviousness relied upon by the Examiner as support  
for the rejection. We have, likewise, reviewed and taken into  
consideration in reaching our decision, Appellants' arguments

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<sup>1</sup> Although the Examiner's statement of the grounds of  
rejection at page 4 of the Answer includes only claims 1-16,  
it is apparent from the record, including the final Office  
action dated April 24, 1996, that claims 1-20, all of the  
pending claims, are included in this appeal. This is  
confirmed by the Examiner's confirmation (Answer, page 2) of  
Appellants' statement of the status of the claims.

<sup>2</sup> The Appeal Brief was filed October 29, 1996. In  
response to the Examiner's Answer dated January 8, 1997, a  
Reply Brief was filed February 28, 1997 which was acknowledged  
and entered by the Examiner without further comment on April  
3, 1997.

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set forth in the Briefs along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 1-3, 11, 14-18, and 20. We reach the opposite conclusion with respect to claims 4-10, 12, 13, and 19. Accordingly, we affirm-in-part.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the Examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966), and to provide a reason why one

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having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the Examiner are an essential part of complying with the burden of presenting a prima facie case of

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obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24  
USPQ2d  
1443, 1444 (Fed. Cir. 1992).

With respect to independent claims 1, 11, 14, and 17, the Examiner has demonstrated (Answer, page 4) how the various claimed circuit chips, storage elements, and transceiver circuits are present in the test device of Sauerwald. As the basis for the obviousness rejection, the Examiner asserts the obviousness to the skilled artisan of integrating the off-chip selector circuitry illustrated, for example, in Sauerwald's Figure 4, within one of the circuit chips 52 and 54.

In response, Appellants attack the Examiner's establishment of a prima facie case of obviousness by asserting (Brief, pages 8-10) that Sauerwald teaches away from on-chip selection circuitry. Appellants point to passages in Sauerwald, directed to a chip self-test feature, which describe the disadvantages and advantages under certain conditions of placing such feature on-chip. Appellants proceed to draw the inference that, since Sauerwald is silent about on-chip self testing for interconnects, there is an implicit teaching away from such feature.

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After reviewing the arguments of record, we are of the view that Appellants' conclusions drawn from the disclosure of Sauerwald are unwarranted. Contrary to Appellants' assertion of "teaching away," it is our view that Sauerwald's discussion of advantages and disadvantages of on-chip testing is nothing more than a recognition that a circuit designer is faced with competing objectives (e.g., speed, size, economy) when deciding to place circuits on-chip or off-chip. We are convinced that the skilled artisan would have found it obvious to arbitrarily locate the externally located selection circuitry illustrated in Figure 4 of Sauerwald to an on-chip location to address particular test circuit performance objectives.

We also find the Examiner's observations at page 7 of the Answer which point to Appellants' lack of disclosure of any advantages resulting from placement of interconnect test selection circuitry at an on-chip location to be persuasive. A review of Appellants' specification reveals that, contrary to the arguments on appeal, Appellants have recognized the arbitrary nature of the location of the interconnection selection circuitry. This is evidenced by Appellants'

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disclosure at page 6, lines 12-14 of the specification which states:

In the example shown in Fig. 1 the selector 120 is integrated in chip 100 but the selector 120 may be a separate circuit component (emphasis added).

As a final argument, Appellants contend (Brief, page 12) that no teaching or suggestion exists in Sauerwald as to how to implement interconnect test selection circuitry on a chip. This is not surprising, however, since Sauerwald admittedly has no explicit disclosure of on-chip implementation of selection circuitry. It is our view, however, that in view of the availability of at least very-large-scale integration (VLSI) techniques at the time of filing of Appellants' application, Appellants' arguments that the skilled artisan would not be able to incorporate selection circuitry on a single semiconductor chip strains credulity.

In view of the above discussion, it is our opinion that the Examiner has established a prima facie case of obviousness which remains unrebutted by any convincing arguments from Appellants. Accordingly, the Examiner's 35 U.S.C. § 103 rejection of independent claims 1, 11, 14, and 17 is sustained.

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Turning to a consideration of dependent claims 2, 3, 15, 16, 18, and 20, we sustain the 35 U.S.C. § 103 rejection of these claims as well. We agree with the Examiner that the transceiver, counter, and decoder circuitry of dependent claims 2, 3, 16, and 18 is suggested by the circuitry illustrated in Figures 5a and 5b of Sauerwald. Similarly, we find that the test pattern and signature register features of claims 15 and 20 are suggested at column 9, lines 28-65 and column 10, lines 60-68, respectively, of Sauerwald.

We next turn to a consideration of dependent claims 4-10, 12, 13, and 19 and note that, while we found Appellants' arguments to be unpersuasive with respect to claims 1-3, 11, 14-18, and 20, we reach the opposite conclusion with respect to dependent claims 4-10, 12, 13, and 19. Dependent claim 4, upon which claims 5-8 depend, 12, 13, and 19 are directed to sensing circuitry which determines the establishment of a data link between data transceivers. While the Examiner recognizes that Sauerwald has no disclosure of such feature, the Examiner nevertheless concludes (Answer, page 5) that the skilled artisan would have found it obvious to provide such a feature. The Examiner, however, has provided no support on the record

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for such a conclusion. Similar lack of support on the record is apparent for the Examiner's conclusion of obviousness with respect to the multiplexing feature of claim 9 and the clock circuitry of claim 10. We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a prior art reference, common knowledge or capable of unquestionable demonstration. Our reviewing court requires this evidence in order to establish a prima facie case. In re Knapp-Monarch Co., 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA 1961); In re Cofer, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966). Therefore, we do not sustain the Examiner's 35 U.S.C. § 103 rejection of dependent claims 4-10, 12, 13, and 19.

In summary, we have sustained the 35 U.S.C. § 103 rejection of claims 1-3, 11, 14-18, and 20, but have not sustained the 35 U.S.C. § 103 rejection of claims 4-10, 12, 13, and 19. Therefore, the Examiner's decision rejecting claims 1-20 is affirmed-in-part.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

|        |                             |   |               |
|--------|-----------------------------|---|---------------|
|        | Lee E. Barrett              | ) |               |
|        | Administrative Patent Judge | ) |               |
|        |                             | ) |               |
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|        | Michael R. Fleming          | ) | BOARD OF      |
| PATENT | Administrative Patent Judge | ) | APPEALS AND   |
|        |                             | ) | INTERFERENCES |
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|        | Joseph F. Ruggiero          | ) |               |
|        | Administrative Patent Judge | ) |               |

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