

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 20

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHIH-WEI D. CHANG, JOEL F. BONEY, and JASPAL KOHLI

Appeal No. 1997-3273
Application No. 08/397,910

ON BRIEF¹

Before KRASS, GROSS, and BLANKENSHIP, Administrative Patent Judges.

GROSS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1, 2, and 4 through 6. We note that appellants indicate on page 2 of the Brief that claim 3 has been cancelled, and we have treated it accordingly.

Appellants' invention relates to a method and apparatus for prioritizing and handling memory errors. The system

¹ We observe that on August 1, 2000 (paper no. 18), appellants filed a waiver of the oral hearing set for September 12, 2000.

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includes a computer in which a memory error address is stored in either a low priority or a high priority error queue, and the computer clock is disabled in response to a detected overflow in the high priority queue. Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A method for prioritizing and handling memory errors in a computer having a memory and a processing unit, the computer operating responsive to a clock, the method comprising the steps of:

detecting the occurrence of a memory error;

identifying the type of memory error as either a first type or a second type;

storing in a first error queue an address of the memory error if the error is a first type of error;

storing in a second error queue an address of the memory error if the error is a second type of error;

detecting an overflow if more than a predetermined number of addresses are stored in the second error queue;

disabling the clock responsive to the detected overflow.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:²

² May, Jr., PN 3,573,745, Giroir et al., PN 4,980,852, and Renault et al., PN 5,471,510, are all cited in the prior art section of the Examiner's Answer but were not applied in any rejection. Therefore, we have not considered them.

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Bartlett 1982	4,321,477	Mar. 23,
Kimmel 1989	4,850,027	Jul. 18,
Bronikowski et al. 1992 (Bronikowski)	5,163,151	Nov. 10,

Claims 1, 2, and 4 through 6 stand rejected under 35 U.S.C. § 103 as being unpatentable over Bronikowski in view of Kimmel.

Reference is made to the Examiner's Answer (Paper No. 14, mailed April 10, 1997) for the examiner's complete reasoning in support of the rejection, and to appellants' Brief (Paper No. 13, filed January 23, 1997) and Reply Brief (Paper No. 15, filed August 6, 1997) for appellants' arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellants and the examiner. As a consequence of our review, we will reverse the obviousness rejection of claims 1, 2, and 4 through 6.

Appellants argue (Brief, pages 8-10) that the examiner has failed to provide appropriate motivation for combining Bronikowski and Kimmel in rejecting the claims and also

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(Brief, page 10) that the prior art fails to show the claimed subject matter. We agree.

Bronikowski is directed to a system for processing and prioritizing alarms, not memory errors. Each alarm is sent to one of three alarm sub-queues according to its severity. (See column 9, lines 37-54, and column 10, lines 23-28).

Bronikowski does not store the addresses of memory errors. Further, Bronikowski states (column 11, lines 9-13) that a standard error code is returned when an alarm is written to an alarm queue which is already full, rather than disabling the clock responsive to the overflow.

The examiner applies Kimmel as showing (Answer, page 6) that it "was notoriously well known in the art" to stop a clock to prevent overflowing a buffer. However, merely that it was well known to stop the clock to prevent overflow of a buffer does not render it obvious to do so in a particular system. For example, Kimmel is directed to an image processing system with data buffers, rather than memory error queues. Kimmel discloses (column 42, line 55-column 43, line 4) stopping the system clock before overflowing the data buffer. However, nothing in Kimmel suggests stopping the

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system clock when an alarm queue is full, since Kimmel is directed to image processing and the status of data buffers. Further, nothing in Kimmel suggests modifying Bronikowski to stop the system clock rather than returning an error code when an alarm queue is full.

Assuming that the two references could be combined, and that the combination included prioritized memory error queues, nothing in either reference suggests only detecting an overflow in the second error queue and stopping the clock responsive to that detection. If one were to combine Kimmel and Bronikowski as proposed by the examiner, the clock would be disabled whenever an overflow condition were detected in any of the queues, not just one of the queues, as pointed out by appellants (Brief, page 10).

In the Answer, the examiner introduced Bartlett as providing further evidence that it was well-known to stop the system clock to prevent overflow. However, as indicated above, merely that it was well-known does not render it obvious for any particular type of system. Accordingly, we find appellants' arguments convincing, and we will reverse the rejection of claims 1, 2, and 4 through 6.

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CONCLUSION

The decision of the examiner rejecting claims 1, 2, and 4 through 6 under 35 U.S.C. § 103 is reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
ANITA PELLMAN GROSS)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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HOWARD B. BLANKENSHIP)	
Administrative Patent Judge)	

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