

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 36

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KEIICHIRO SHIMADA,
KATSUMI MATSUNO,
and SUNAO FURUI

Appeal No. 1997-3911
Application Serial No. 08/368,758¹

ON BRIEF

Before THOMAS, MARTIN, and BARRETT, Administrative Patent
Judges.

MARTIN, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134 from the
examiner's final rejection of claims 14-20, 22, and 23, all of

¹ Application for patent filed January 4, 1995, as a
continuation of Serial No. 07/882,268, filed May 13, 1992.

Appeal No. 1997-3911
Application 08/368,758

the pending claims, under 35 U.S.C. § 103.² We affirm-in-part.

The invention

The invention relates to correcting errors or bugs discovered in the information such as programs and data stored as firmware in the ROM of a mass-produced micro-controller without requiring replacement of the ROM (Spec. at 1, line 20 to p. 2, line 24). Appellants' micro-controller is designed to permit correction information to be entered into the RAM of the micro-controller for use in place of the erroneous information stored in the ROM.

As explained in the specification at page 5, lines 7-33, appellants' Figure 1 shows an electronics apparatus 1 which, in addition to the ROM 15, input means 12, data bus 13, address controller 14, and address bus 16 found in a conventional micro-controller, contains correcting information storing means 100 and switching means 200 responsive to correcting information provided by external storage means 11.

² The Final Rejection (Paper No. 20) incorrectly gives the claim numbers as 14-23.

The correcting information storing means 100 includes (a) a correcting address storing unit 3 for storing the starting addresses of defective portions of ROM 15 and (b) a correcting content storing unit 2 for storing correcting information therein, including the ROM addresses to be accessed after the respective correcting operations have been completed. The writing of the correcting information into the correcting information storing means 100 is carried out by a loader within ROM 15 when the electronics apparatus 1, for example, is initialized (Spec. at 6, lines 1-4). While the external storage means 11 is shown outside the electronics apparatus 1, it may be provided within the electronics apparatus 1 (Spec. at 6, lines 5-7). The switching means 200 includes an address comparing unit 4 and an access altering unit 6. The operation of the correction circuitry is described as follows at page 6, lines 15-34:

The address controller 14, e.g. a CPU[,] controls the address of the ROM 15 through the address bus 16. When the address controller 14 reaches the correcting address of the defective portion, two addresses input to the comparing unit 4, i.e., an execution address from the address bus 14 and a correcting address from the correcting address storing unit 3, become equal and hence the comparing unit 4 outputs an address coincidence signal 5 to the access altering unit 6. The access

altering unit 6 sends information to the address controller 14 to cause the address control to address the correcting content storage unit 2 instead of the ROM 15.

After the correction content stored in the correcting content storage section 2 is executed, the address control of the address controller 14 is returned to the address at which the defective portion in the ROM 15 designated by the correcting content is skipped.

Figure 2 shows an embodiment in which the correcting address storing unit 3 of Figure 1 is implemented as a register 21 and the correcting content storing unit 2 of Figure 1 is implemented as part of the RAM 26 (Spec. at 7, lines 20-25). Furthermore, the leading address of the correcting content stored in the RAM 26 is latched in the interruption vector register 23b when the correcting information is written (Spec. at 8, lines 18-21). A control flag latch 23a stores a "1" or a "0" to indicate whether or not correction information has been entered into register 21 and RAM 26 (Spec. at 8, lines 4-9). If the answer is yes, the control flag latch closes gate 24 to permit any subsequently generated coincidence signals 5 to be applied to the input of interruption control circuit 25, thereby causing control by the CPU 14 to be moved to the address shown by the interruption register 23b (Spec. at 8, lines 9-17). The end

of the correcting content stored in the RAM 26 is a jump instruction for skipping the defective portion of the ROM 15 before returning control from RAM 26 to ROM 15 (Spec. at 8, lines 26-30). The initialization procedure is depicted by Figure 3, which is a flow chart showing that

[u]pon initialization after the electronics apparatus is powered, using the correcting information stored in the EEPROM 27, the correcting address is latched in the interruption generating address register 21 by the initial patch loader stored in the ROM 15 at step ST1. The leading address of the correcting content is latched in the interrupt vector register 23b in step ST2. Further, the correcting content is written in a predetermined address of the RAM 26 and the control flag latch 23a is set to "1" at step ST3. [Spec. at 9, lines 5-15.]

The claims

Claim 14, the sole independent claims on appeal, reads as follows:

14. A micro-controller integrated on a single substrate and in which [sic, including?] a read-only information storage means for storing firmware, address control means for performing address control, and input means for inputting information supplied thereto from a source external to the substrate, the micro-controller comprising:

random access correcting information storage means located on the single substrate for receiving correcting information input thereto from the source external to the substrate through the input means and storing the correcting information upon any initialization of the micro-controller,

Appeal No. 1997-3911
Application 08/368,758

wherein the correcting information is indicative of modifications for all defective information parts stored in the read-only information storage means; and

switching means located on the single substrate for selectively switching the access by the address control means from the defective information part in the read-only information storage means to the correcting information in the correcting information storage means.

The references and grounds of rejection

The references named in the two grounds of rejection are:

Patrick et al. (Patrick) Sept. 17, 1985	4,542,453	
Yamaguchi et al. (Yamaguchi) Sept. 24, 1991	5,051,897	
Takahashi 31, 1983 (Japanese patent application)	58-16350	Jan.

Consistent with the examiner and appellants, we will refer to the Takahashi reference as "Denki," which is the name of the applicant rather than the name of the inventor. Our understanding of this reference is based on a translation (copy attached) obtained by the PTO after the Notice of Appeal was filed.

Claims 14-20, 22, and 23 stand rejected under § 103 for obviousness over Denki.

Appeal No. 1997-3911
Application 08/368,758

Claims 14-20, 22, and 23 alternatively stand rejected under § 103 for obviousness over Yamaguchi in view of Patrick.

The Answer (at 3-4) also lists D.P. Siewiorek et al., Computer Structures: Principles and Examples 581, 612-14 (1982) as part of the "prior art of record relied upon in the rejection of claims under appeal." This reference was not mentioned in the final rejection and is entitled to no consideration because it is not mentioned in the statement of either rejection. See Ex parte Movva, 31 USPQ2d 1027, 1028 n.1 (Bd. Pat. App. & Int. 1993):

The examiner has cited and relied upon four new references in the Examiner's Answer but did not make a new ground of rejection. As set forth in In re Hoch, 57 CCPA 1292, 428 F.2d 1341, 166 USPQ 406 (1970), "[W]hen a reference is relied on to support a rejection, whether or not in a 'minor capacity,' there would appear to be no excuse for not positively including the reference in the statement of rejection." The failure of the examiner to do so here appears to be for the purpose of avoiding a new ground of rejection. Since a new ground of rejection was not made, appellants were not entitled as a matter of right to respond to this new evidence of obviousness by way of amendment and/or evidence. Rather, appellants were limited to presenting argument by way of a Reply Brief. The procedural disadvantage in which appellants were placed by the examiner's action is apparent. Accordingly, we have not considered the four references in determining the correctness of the rejection before us in this appeal. If in further prosecution of this subject

Appeal No. 1997-3911
Application 08/368,758

matter, the examiner continues to find these references to be relevant evidence of obviousness (see n. 6, infra), a proper rejection should be made.

Accord Ex parte Hiyamizu, 10 USPQ2d 1393, 1394 (Bd. Pat. App. & Int. 1988); In re Raske, 28 USPQ2d 1304, 1304-05 (Bd. Pat. App. & Int. 1993). See also MPEP § 706.02(j) (7th ed., rev. 1, Feb. 2000)) ("Where a reference is relied on to support a rejection, whether or not in a minor capacity, that reference should be positively included in the statement of the rejection. See

In re Hoch, 428 F.2d 1341, [1342] n.3, 166 USPQ 406, [407] n.3 (CCPA 1970)."). For the same reason, we will not consider Heene U.S. Patent No. 4,802,119, which is discussed in the Examiner's Answer at 5 but not mentioned in either statement of rejection.

The Answer (at 4) identifies J.M. Rosenberg, Dictionary of Computers, Information Processing & Telecommunications 94, 239, 292, 301, 327, 382, 394, 613 (2d ed. 1987), as "New Prior Art."

Appeal No. 1997-3911
Application 08/368,758

Because appellants do not take issue with the examiner's reliance on the definitions in this dictionary, those definitions may be considered, if necessary.

Grouping of claims

Appellants treat dependent claims 15-17, 19, 20, 22, and 23 as standing or falling with claim 14 and argue claim 18 separately (Brief at 5).

The level of skill in the art

The level of skill in the art is represented by the references. In re Oelrich, 579 F.2d 86, 91, 198 USPQ 210, 214 (CCPA 1978) ("the PTO usually must evaluate both the scope and content of the prior art and the level of ordinary skill solely on the cold words of the literature"). In re GPAC Inc., 57 F.3d 1573, 1579, 35 USPQ2d 1116, 1121 (Fed. Cir. 1995) (Board did not err in adopting the approach that the level of skill in the art was best determined by the references of record).

Appellants' burden of proof on appeal

In re Rouffet, 149 F.3d 1350, 1355, 47 USPQ2d 1453, 1455 (Fed. Cir. 1998), explains that

Appeal No. 1997-3911
Application 08/368,758

[t]o reject claims in an application under section 103, an examiner must show an unrebutted prima facie case of obviousness. See In re Deuel, 51 F.3d 1552, 1557, 34 USPQ2d 1210, 1214 (Fed. Cir. 1995). In the absence of a proper prima facie case of obviousness, an applicant who complies with the other statutory requirements is entitled to a patent. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). On appeal to the Board, an applicant can overcome a rejection by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobviousness. See id.

The rejection based on Yamaguchi in view of Patrick

Yamaguchi, like appellants, is concerned with correcting errors or bugs in the programming commands stored in the ROM of a mass-produced microcomputer without requiring replacement of the ROM (col. 1, lines 7-12 and 48-53). The correction information is stored in a PROM (programmable read-only memory) 6 and is used in place of the erroneous information contained in mask ROM 1 when coincidence circuit 8 detects a match between the address generated by the programmable counter PC 3 in CPU 2 and one of the ROM addresses stored in register 7, which represent the addresses of erroneous ROM information. All of these elements, including the PROM, are mounted on a single chip

Appeal No. 1997-3911
Application 08/368,758

(col. 1, line 54 to col. 2, line 5), i.e., on a single substrate.

In arguing that it would have been obvious to replace PROM 6 with a RAM (Final Rej. at 5-6; Answer at 10), the examiner appears to believe that the phrase "random access correcting information storage means" in claim 14 does not read on Yamaguchi's PROM 6. This view appears to be shared by appellants, who argue that "[Yamaguchi's] correcting information storage means (i.e., programmable ROM 6) is a one-time programmable ROM rather than a '**random access** correcting information storage means' as recited in claim 14" (Brief at 11-12). In our opinion, the phrase "random access correcting information storage means" is broad enough to read on Yamaguchi's PROM 6. As explained in In re Morris, 127 F.3d 1048, 1054, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997),

the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification.

While a RAM (random access memory) and a PROM are distinguishable on the basis of volatility,³ appellants' specification does not define the phrase "random access correcting information storage means" to mean a RAM, with the result that the phrase is broad enough to read on Yamaguchi's PROM 6. Consequently, it is necessary to consider whether PROM 6 also satisfies the two additional limitations claim 14 places on the random access correcting information storage means. The first limitation, i.e., that the random access correcting information storage means "receiv[es] correcting information input thereto from the source external to the substrate through the input means," is satisfied because the

³ See TechEncyclopedia,
<http://techweb.com/encyclopedia/defineterm?term=ram:>

RAM -

(**R**andom **A**ccess **M**emory) A group of memory chips, typically of the dynamic RAM (DRAM) type, which functions as the computer's primary workspace. . . . The "random" in RAM means that the contents of each byte can be directly accessed without regard to the bytes before or after it. This is also true of other types of memory chips, including ROMs and PROMs. However, unlike ROMs and PROMs, RAM chips require power to maintain their content, which is why you must save your data onto disk before you turn the computer off.

[June 15, 2000.] [Copy enclosed.]

correction information is written into PROM 6 via the input/output port 12. See column 3, lines 23-26 ("A corrected instruction thus is written in a particular address of the PROM 6 as the destination of the interruption via the I/O port 12 (STEP S10), so that the microcomputer executes the corrected program.").⁴

The second limitation is that the random access correcting information storage means "stor[es] the correcting information upon any initialization of the micro-controller." The examiner describes Yamaguchi as not teaching this limitation (Answer at 5, lines 5-7), for which he relies on Patrick, discussed infra. We agree that Yamaguchi does not teach storing the correction information in PROM 6 upon any initialization of the micro-controller, which we understand to mean that the correction information is re-entered into the random access correcting information storage means every time the operating system or other program is initially loaded.

⁴ The examiner's observation that Yamaguchi fails to teach the use of external storage (Final Rej. at 5) is irrelevant to claim 14, which does not require external storage. That requirement appears in dependent claim 19, which is not separately argued.

Appeal No. 1997-3911
Application 08/368,758

See Rosenberg, Dictionary of Computers, Information Processing & Telecommunications 292, which defines "initial program loader" to mean "the utility routine that loads the initial part of a computer program, such as an operating system or other computer program, so that the computer program can then proceed under its own control." Because Yamaguchi's PROM 6 is non-volatile, the correction data stored therein need not be and is not re-entered during subsequent initializations of the either the operating system or a program to be run by the micro-controller.

Appeal No. 1997-3911
Application 08/368,758

As Yamaguchi's PROM 6 therefore fails to satisfy all of claim 14's limitations on the random access correcting information storage means, it is necessary to consider the examiner's case for substituting a RAM for Yamaguchi's PROM 6, which relies in part on Patrick. The examiner explains:

As per the use of storing correcting information within a RAM, it is a well known functional equivalent to storing [sic] the information in other storage devices (i.e. PROM, ROM, EEPROM etc.). It would have been obvious to one of ordinary skill in the art at the time of the invention, to replace the Prom [sic, PROM] of Yamaguchi with a RAM for storing correcting data. This modification would have been obvious to one of ordinary skill because, they are well known functional equivalents for storing data, and [it] involves only rudimentary skill in the art to perform such a modification. And further because, Patrick provides the motive of storing correction data on a more cost effective RAM. [Final Rej. at 5-6.]

The Answer further states (at 10) that replacing Yamaguchi's PROM 6 with a RAM "would have been obvious to one of ordinary skill in the art as each device is a matter of design choice, and further either would be applicable for the act of storing data in a computer system." We will first address Patrick. Patrick, like appellants and Yamaguchi, is concerned with correcting errors or bugs in the programming commands stored in the ROM (17) of a mass-produced microcomputer (10) without

requiring replacement of the ROM (col. 1, lines 63-68). Referring to Figure 1, Patrick employs a program patching module 16 which is connectable to but is not part of the microcomputer chip 10. This module includes a patch control memory 44 having one bit for each memory address in the on-chip ROM program store 17; the bit in memory 44 associated with each address of the ROM 17 is set to a 1 or 0 depending upon whether or not a patch is to be implemented beginning at the next address (col. 5, lines 12-16). Patch memory 40 is a programmable memory (PROM) containing instruction words to supplement or replace instructions stored in the ROM 17 (col. 4, lines 45-49; col. 6, lines 10-13). Patch control memory 44 is described as "a standard 'X1' memory commercially available at low cost" (col. 5, lines 62-64). Furthermore, in its "simplest embodiment" memory 44 is a PROM or EPROM (col. 6, lines 3-7). Alternatively, memory 44

may be a static RAM, in which case the patch point bits are set by a start-up routine when the system is reset or initialized [sic]. This routine may be programmed into the PROM 40 and accessed as part of the reset procedure originally coded in ROM 17. This coded data from the PROM 40 in the reset procedure generates the data to be written into the RAM 44 by an algorithm (so that excessive space in the PROM 40 is not used up); write inputs 50 to the

memory 44 from the data bus 14 and the control bus 15 provide the write enable command and the one-bit data input for this purpose. [Col. 6, lines 8-19).

In a second embodiment of the invention, shown in Figure 3, a single patch memory 54 performs the functions of memories 40 and 44 of Figure 1 (col. 6, lines 20-22).

The examiner's contention that Patrick generally suggests replacing a ROM with a "more cost effective RAM" (Final Rej. at 6) is incorrect, as should be evident from Patrick's above-noted description of the standard "X1" memory embodiment (presumably not a RAM) as obtainable at "low cost" and his description of the ROM/PROM embodiment as the "simplest embodiment." Be that as it may, Patrick clearly teaches that either a PROM or a RAM can be used to implement his memory 44. However, this teaching appears to be limited to implementing off-chip memory 44 as an off-chip PROM or an off-chip RAM, whereas claim 14 requires an on-chip RAM. Although Patrick discloses an on-chip RAM 18, he does not indicate that it can be used to store the correction information stored in memory 44. Furthermore, Patrick's memory 44, even if implemented as an on-chip RAM, would not store the type of correction information required to satisfy claim 14. The claim, by

calling for the switching means to "selectively switch[] the access by the address control means from the defective information part in the read-only information storage means to the correcting information stored in the correcting information storage means," clearly requires that the correcting information stored in the correcting information storage means be the information that is to be substituted for the defective information. In Patrick, that information is stored in PROM 40 rather than in memory 44, which instead stores one-bit data identifying the ROM addresses of defective information. As Patrick's memories 40 and 44 correspond respectively to Yamaguchi's PROM 6 and register 7, the effect of applying Patrick's RAM suggestion to Yamaguchi would be to replace Yamaguchi's register 7 rather than PROM 6 with a RAM, which would not satisfy the claim.

The rejection is also unconvincing to the extent it is based on the assertions that replacement of Yamaguchi's on-chip PROM 6 with an on-chip RAM would have been obvious because they are "functional equivalents" and that choosing one or the other is therefore a matter of "design choice. The examiner has not explained, and it is not apparent to us, why

one skilled in the art would have replaced the non-volatile storage provided by Yamaguchi's PROM 6 with volatile RAM storage that would require initialization every time the microcomputer is activated. If the PROM is replaced by a RAM, where would the data required for initializing the RAM be stored?

The rejection of claim 14 based on Yamaguchi in view of Patrick is therefore reversed, as is the rejection of dependent claims 15-20, 22, and 23 over those references.

The rejection based on Denki

Denki's invention, like appellants', is concerned with correcting errors or bugs in the programming commands stored in the ROM (1) of a mass-produced microcomputer without requiring replacement of the ROM (Transl. at 3-4). In Denki's system, the correct commands are stored in a substitute command register 5 (transl. at 5). An address comparing circuit 4 compares the addresses generated by microaddress controller circuit 3 to the addresses stored in address comparing circuit 4, which represent the addresses of the erroneous instructions in the ROM (Transl. at 4-5). The commands read out of the ROM are stored in microcommand

register 6. In response to a substitution indicating signal 9 from address comparing circuit 4, the command select circuit 7 selects the substitute command from substitute command register 5 in place of the ROM command stored in microcommand register 6. The output of command select circuit 7 is applied to command determination control circuit 8.

Figure 2 shows the address comparing circuit 4 implemented as a plurality of registers 41a-41c, address comparators 42a-42c, and an OR gate 43, and shows the substitute command register 5 implemented as a plurality of registers 51a-51c. However, Denki also explains that "[t]he registered address registers (41a), (41b) and (41c) may be a RAM or a switch setting system instead of registers. Similarly, the substitution command registers (51a), (51b) and (51c) may also be replaced by a RAM or a switch setting system" (Transl. at 8, lines 1-5). Appellants do not deny that elements 51a-51c implemented as a RAM constitute "random access correcting information storage means" in the sense of claim 14. Instead, they deny that it would have been obvious to (1) locate the RAM "on the single substrate" or (2) store the substitute commands therein "upon any initialization of

Appeal No. 1997-3911
Application 08/368,758

the micro-controller," as required by claim 14. We agree with the examiner that both of these modifications would have been obvious. Considering first the "on the single substrate" limitation, Denki's explanation that "the address comparing circuit (4) or the substitution command register (5) may be provided on a portable external liquid [sic], which is connected to the microprogram control device only when it is needed" makes it clear that these elements alternatively may be internal components of the microprogram control device, as apparently shown in Denki's Figure 1. We hereby take official notice of the fact that it was known at the time the application was filed to form as many components of a mass-produced computerized control circuit as possible on a single substrate in order to reduce the size and cost of the control circuit and that a RAM was known to be one such component.

Compare In re Raynes, 7 F.3d 1037, 1040, 28 USPQ2d 1630, 1631-32 (Fed. Cir. 1993):

In In re Taylor, 288 F.2d 950, 954, 129 USPQ 269, 272 (CCPA 1961), the court referred to broad concepts "in the realm of the obvious", a designation that is apt in this case, for the use of video to display programming and other information is so ubiquitous as to warrant judicial notice. Cf. In re Howard, 394 F.2d 869, 870, 157 USPQ 615,

Appeal No. 1997-3911
Application 08/368,758

616 (CCPA 1968) (taking judicial notice of retail price marking procedures).

Compare also In re Fox, 471 F.2d 1405, 1407, 176 USPQ 340, 341 (CCPA 1973) ("As did the board, we will take judicial notice of the fact that tape recorders commonly erase tape automatically when new 'audio information' is recorded on a tape which already has a recording on it."). Moreover, appellants' specification concedes as much in its "Description of Related Art":

Conventional electronics apparatus such as a video cassette recorder (VCR) having a built-in camera, for example, have mounted thereon a custom LSI (large scale integration) integrated electronics apparatus on one chip as control means, i.e., a so-called micro-controller for controlling the entirety or part of the electronics apparatus.

The micro-controller is an exclusive-use microcomputer which is composed of a central processing unit (CPU), a memory such as a read-only memory (ROM) and a random access memory (RAM) and a peripheral circuit such as an input/output (I/O) port or the like. The CPU acts as an address controller to control the access to the memories or the like or acts as a processor to execute a program. Information such as programs, data and so on for controlling the mounted electronics device are stored in the ROM in the form of firmware. The RAM provides the CPU with a working area or the like to execute a program and the peripheral circuit is used to communicate with the external circuits. Accordingly, mass-production is indispensable for providing inexpensive custom LSI electronics

Appeal No. 1997-3911
Application 08/368,758

apparatus such as micro-controllers or the like.
[Spec. at 1, line 13 to p. 2, line 4.]

Consequently, we agree with the examiner that it would have been obvious, for the purpose of minimizing the size and cost of Denki's microcomputerized control device, to form Denki's substitute command register, when implemented as an internal RAM, on the same substrate as other components of the device.

As for the initialization requirement, re-entry of the substitution commands into Denki's RAM is clearly necessary any time the micro-controller is initialized, which is broad enough to refer to initializing the micro-controller either by loading the operating system or by loading the particular program which requires the substitution commands.

The rejection of claim 14 over Denki is therefore affirmed, as is the rejection of dependent claims 15-17, 19, 20, 22, and 23 over that reference.

The rejection of dependent claim 18 is reversed. Denki does not disclose or suggest means for gating the address coincidence signal 9 only when a control flag latch is set to indicate that there is a defective information part in the read-only information storage means.

Appeal No. 1997-3911
Application 08/368,758

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

)	
JAMES D. THOMAS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOHN C. MARTIN)	
Administrative Patent Judge)	APPEALS AND
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)	INTERFERENCES
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Appeal No. 1997-3911
Application 08/368,758

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Appeal No. 1997-3911
Application 08/368,758