

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte IWAO YAMAMOTO
and
KATSUMI MATSUNO

Appeal No. 1997-4061
Application 08/469,498¹

ON BRIEF

Before THOMAS, HAIRSTON and FLEMING, **Administrative Patent Judges**.

FLEMING, **Administrative Patent Judge**.

¹ Application for patent filed June 6, 1995. According to Appellants, the application is a continuation of Application 08/004,932, filed January 15, 1993, abandoned.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 13 through 20, all of the claims pending in the application. Claims 1 through 12 have been cancelled.

The invention relates to a method and apparatus for patching a program, where the program is fixed in a read-only memory. In particular, Appellants' invention is directed to the problem of patching portions of the program that are executed nonsequentially in that they may be interrupted by an interrupt processing routine. Appellants' invention provides for saving the patching context during the execution of an interrupt processing routine and for restoring the patching context at the termination of the execution of the interruption processing routine.

Independent claim 13 is reproduced as follows:

13. An electronic computing apparatus comprising:

- (a) a data bus;
- (b) an address bus;

(c) a read-only memory connected for providing to the data bus, under control of a read-only memory address on the address bus, an instruction held in the read-only memory at a location designated by the read-only memory address, said read-only memory having a plurality of locations that hold a plurality of program instructions, said plurality of program instructions

collectively comprising a program including a plurality of interrupt processing routines;

(d) a processor, connected to said data bus and said address bus, that executes the program instructions;

(e) address control means responsive to the program instructions executed by the processor for providing to the address bus the read-only memory addresses of said plurality of locations holding the program instructions to be executed by the processor;

(f) a patch information memory for holding a plurality of patch instructions representing a plurality of modifications to execution of the program by the processor, said patch information memory connected for providing to the data bus, under control of a patch memory address on the address bus, a patch instruction held in the patch information memory at a location designated by the patch memory address on the address bus;

(g) switching means including a first switching means memory, the switching means for providing to the address bus, under the control of first control data held in the first switching means memory, a patch memory address of a first plurality of patch instructions in said patch information memory in place of a read-only memory address of instructions of a first bug portion of the program, such that the first plurality of patch instructions are provided to the processor

for execution in place of the instructions of the first bug portion, whereby said first plurality of patch instructions are executed by the processor in place of the instructions of the first bug portion, said switching means further including

i) a second switching means memory;

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the
processor, the first control data into the second switching means memory, and for thereafter storing second control data into said first switching means memory and such that, during said one of said plurality of interrupt processing routines, the switching means

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provides to the address bus, under the control of second control data held in the first switching memory, a patch memory address of a second plurality of patch instructions in said patch information memory in place of a read-only memory address of instructions of a second bug portion of the program, such that the second plurality of patch instructions are provided to the processor for execution in place of the instructions of the second bug portion, whereby, during said one of said plurality of interrupt processing routines, said second plurality of patch instructions are executed by the processor in place of the instructions of said second bug portion; and

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iii) means for restoring, at a termination of execution of said one of said plurality of interrupt processing routines by the processor, the first control data held in the second switching means memory into the first switching means memory

wherein said first control data includes a first portion which consists of the read-only memory address of the first bug portion and a second portion which consists of the patch memory address of the first plurality of patch instructions, and wherein the second control data includes a first portion which consists of the read-only memory address of the second bug portion and a second portion which consists of the patch memory address of the second plurality of patch instructions.

The references relied on by the Examiner are as follows:

Fairchild et al. (Fairchild)	4,296,470	Oct. 20, 1981
Clarke (European Patent Application)	0,458,559	Nov. 27, 1991

Claims 13 through 20 stand rejected under 35 U.S.C. § 103 as being unpatentable over Clarke and Fairchild.

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Rather than repeat the arguments of Appellants or the Examiner, we make reference to the briefs² and the answer for the details thereof.

OPINION

After a careful review of the evidence before us, we agree with the Examiner that claims 13 through 15 and 17 through 20 are properly rejected under 35 U.S.C. § 103. Thus, we will sustain the rejection of these claims but we will reverse the rejection of claim 16 on appeal for the reasons set forth *infra*.

At the outset, we note that Appellants state on page 4 of the brief that claims 13 through 15 and 18 through 20 stand or fall together and claim 16 stands by itself. We note that Appellants argue claims 13 through 15 and 18 through 20 as a single group and claim 16 separately in the brief.

² Appellants filed an appeal brief on January 2, 1997. Appellants filed a reply brief on May 7, 1997. The Examiner mailed a communication on May 21, 1997 stating that the reply brief has been entered and considered but no further response by the Examiner is deemed necessary.

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37 CFR § 1.192(c)(7) (July 1, 1995) **as amended at**
60 Fed. Reg. 14518 (March 17, 1995), which was controlling at
the time of Appellants' filing the brief, states:

For each ground of rejection which appellant contests and which applies to a group of two or more claims, the Board shall select a single claim from the group and shall decide the appeal as to the ground of rejection on the basis of that claim alone unless a statement is included that the claims of the group do not stand or fall together and, in the argument under paragraph (c)(8) of this section, appellant explains why the claims of the group are believed to be separately patentable. Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable.

We will, thereby, consider Appellants' claims 13 through 15 and 18 through 20 as a single group as standing or falling together and we will treat claim 13 as a representative claim of that group. In addition, we will consider Appellants' claim 16 separately.

On pages 3 and 4 of the Examiner's answer, the Examiner argues that Clarke discloses all the features of

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Appellants' invention as set forth in claim 13 except for storing the first control data from the first switching means memory into the second switching means memory and restoring means for restoring

first control data back into the first switching means memory. The Examiner relies on Fairchild for disclosing this feature. In particular, on page 4 of the answer, the Examiner states that Fairchild shows that the address of an instruction address register (IAR)(24) is transferred into a storage address register (SAR)(26) for the purposes of addressing the instruction in the main storage unit (21) to be executed. The Examiner further points out that when an interrupt occurs, the contents of the IAR 24 are saved in an interrupt link register (ILR)(170) and when the interrupt routine is finished, the contents of ILR 170 are transferred back into the SAR. The Examiner points to Fairchild, column 2, lines 31 through 46; column 3, lines 52 through 62; and column 8, line 66, through

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column 9, line 59. The Examiner argues that it would have been obvious to one of ordinary skill in the art to modify the Clarke patch system to use the Fairchild system of handling interrupt routines so that a moving means for storing the first control data from the first switching means memory into the second switching means memory and restoring the means for restoring the first control data back into the first switching means memory is accomplished.

Appellants argue on pages 5 through 7 of the brief that incorporating the Fairchild teaching into the Clarke system would not yield Appellants' claimed invention. In particular, Appellants argue that Appellants' claim 13 recites "control data" and this is not the same as what is held in Fairchild's instruction link register.

We note that Appellants' claim 13 recites "means for moving, during execution of one of said plurality of interrupt

processing routines by the processor, the first control data into the second switching means memory." Furthermore, Appellants' claim 13 recites a switching means under the control of first control data held in the first switching means memory.

Fairchild teaches in column 8, line 66, through column 9, line 9, that when an interrupt occurs, the contents of IAR 24 together with paging information stored in page latches 162 and arithmetic and logic unit (ALU) status bits of ALU status latches 120, 122 and 124 are saved into ILR 170. We find that the information stored into ILR 170 meets Appellants' claimed language "control data" and thereby reads on Appellants' limitations recited in claim 13.

Appellants also argue that it is not clear what would motivate one skilled in the art to incorporate the Fairchild link registers into the Clarke system. In particular, Appellants point out that Fairchild discloses a pre-fetch processor and that Clarke does not disclose a pre-fetch processor and, at

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best, if one skilled in the art were considering modifying Clarke in view of Fairchild, he would be led to wholly incorporate Fairchild's pre-fetch mechanism, including link registers and link latch circuits, so that the Clarke processor could efficiently execute instructions in a pipeline fashion.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). The Federal Circuit reasons in ***Para-Ordnance Mfg. Inc. v. SGS Importers Int'l Inc.***, 73 F.3d 1085, 1088-89, 37 USPQ2d 1237, 1239-40 (Fed. Cir. 1995), ***cert. denied***, 519 U.S. 822 (1996), that for the determination of obviousness, the court must answer whether one of ordinary skill

in the art who sets out to solve the problem and who had before him in his workshop the prior art, would have been

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reasonably expected to use the solution that is claimed by the Appellants.

We agree with the Appellants that Fairchild does teach the concept of pipeline processors. However, we also find that Fairchild teaches another concept, --- the use of IARs to store control data when an interrupt occurs so that the processor may start exactly where it was before it was interrupted. We find that this concept would have suggested to those skilled in the art to use it as a solution in the Clarke system so that the Clarke system will be able to return to the patch program whenever an interrupt occurs. Therefore, we find that Fairchild would have suggested the desirability of modifying the Clarke system so that the Clarke system would be able to process patch programs even when an interrupt routine occurs. Therefore, we will sustain the Examiner's rejection of claims 13 through 15 and 17 through 20 under 35 U.S.C. § 103 as being unpatentable over Clarke and Fairchild.

On pages 8 and 9 of the brief, Appellants argue that neither Fairchild nor Clarke suggests comparing means that compares addresses on the address bar, the first portion of

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whichever of said first and second control data is in the first switching means memory. Appellants argue that claim 16 recites an "interrupt signal generating means for generating an interrupt to said processor to cause the processor to execute a patch processing interrupt routine." Appellants argue that nothing is either disclosed or suggested by Clarke or Fairchild of an interrupt signal generating means for generating an interrupt to said processor to cause the process to execute a patch processing routine.

We note that the Examiner has not responded to Appellants' argument in the Examiner's answer. Upon our review of Clarke and Fairchild, we fail to find any teaching or suggestion of this limitation. Therefore, we will not sustain the Examiner's rejection of claim 16 under 35 U.S.C. § 103.

In view of the foregoing, the decision of the Examiner rejecting claims 13 through 15 and 17 through 20 under 35 U.S.C. § 103 is affirmed; however, the decision of the Examiner rejecting claim 16 under 35 U.S.C. § 103 is reversed.

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No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

	JAMES D. THOMAS)	
	Administrative Patent Judge)	
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PATENT)	BOARD OF
	KENNETH W. HAIRSTON)	APPEALS AND
	Administrative Patent Judge)	INTERFER-
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	MICHAEL R. FLEMING)	
	Administrative Patent Judge)	

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MRF:psb

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Alan S. Hodes
Limbach & Limbach
2001 Ferry Building
San Francisco, CA 94111