

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ARMIN REINMUTH

Appeal No. 1997-4120
Application No. 08/347,341¹

ON BRIEF

Before HAIRSTON, MARTIN, and BARRY, Administrative Patent Judges.

BARRY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the final rejection of claims 4-6. We reverse.

¹ The application was filed December 6, 1994 under 35 U.S.C. § 371 base on PCT/DE93/00471 filed June 1, 1993.

BACKGROUND

The invention at issue in this appeal relates to synchronizing processors. In systems having multiple processors that process related tasks and exchange data with each other, processing must be synchronized. The invention synchronizes changes in the state of operation of the processors and ensures that the processors execute jobs synchronously. According to the invention, the first processor to reach a synchronization point while executing a process enters a data set into a common storage area. Interrupt controllers associated with the processors detect the entry and send interrupt signals to the processors to initiate a synchronous job or to change the processors' state of operation.

Claim 4, which is representative for our purposes,
follows:

4. A computer system comprising:

a plurality of interconnected processors;

a plurality of memories each one associated with one of said interconnected processors, each having a common storage area to which each of said processors have write access;

a plurality of interrupt controllers, each one associated with one of said processors;

wherein, to synchronize changes in the state of operation of the processors and/or to handle processor jobs in a synchronous manner, a data set is able to be entered into said common storage area of each of said plurality of memories by the processor that first reaches a predetermined synchronization point during execution of a process;

wherein said interrupt controllers detect a change in said data set, said controllers providing interrupt signals that are fed to said processors, through which means, according to an identifier in the entry in the common storage area, a change in the state of operation of said processors and/or a synchronous job processing is able to be initiated; and

means for indicating to said processors whether the synchronization of a change in the state of operation or the synchronization of processor job [sic] is time-critical or non-time-critical.

The references relied on by the patent examiner in
rejecting the claims follow:

Kametani 1994	5,361,369	Nov. 1, (filed Sept. 13, 1991)
Papadopoulos et al. (Papadopoulos) 1995	5,430,850	July 4, (filed July 22, 1991).

Claims 4-6 stand rejected under 35 U.S.C. § 103 as
obvious over Kametani in view of Papadopoulos. Rather than
repeat the

arguments of the appellant or examiner in toto, we refer the reader to the appeal and reply briefs and the examiner's answer for the respective details thereof.

OPINION

In reaching our decision in this appeal, we considered the subject matter on appeal and the rejection and evidence advanced by the examiner. We also considered the arguments of the appellant and examiner. After considering the record before us, we cannot say that the evidence and level of skill in the art would have suggested the invention of claims 4-6. Accordingly, we reverse.

We begin our consideration of the claims by recalling that in rejecting claims under 35 U.S.C. § 103, the patent examiner bears the initial burden of establishing a prima facie case of obviousness. A prima facie case is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of

ordinary skill in the art. If the examiner fails to establish a prima facie case, an obviousness rejection is improper and will be overturned. In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). With this in mind, we address the appellant's arguments.

Regarding the obviousness of claim 4, the appellant argues, "[s]ynchronization is carried out by the synchronous processing circuit 101 of Fig. 1 [of Kametani], and it is not clear from the reference that this circuit relies on the contents of a common storage area as required by independent claim 4 of the present application." (Appeal Br. at 5.) He also argues that Papadopoulos "fails to disclose the processor/common storage area/interrupt controller configuration which is the subject matter of the present application." (Reply Br. at 3.)

In response, the examiner opines that the claim language "does not indicate that the data set or common storage area is

used to synchronize the processors by performing any time
delay or stalling of processors but merely that at some point

a

processor writes to the common storage area and all the processors see an identical value in some portion of the data set concurrently." (Examiner's Answer at 6.)

We cannot find that Kametani and Papadopoulos teach or would have suggested the "wherein" clauses of claim 4. The claim recites in pertinent part the following limitations:

wherein, to synchronize changes in the state of operation of the processors and/or to handle processor jobs in a synchronous manner, a data set is able to be entered into said common storage area of each of said plurality of memories by the processor that first reaches a predetermined synchronization point during execution of a process;

wherein said interrupt controllers detect a change in said data set, said controllers providing interrupt signals that are fed to said processors, through which means, according to an identifier in the entry in the common storage area, a change in the state of operation of said processors and/or a synchronous job processing is able to be initiated
....

In short, the claim specifies that when one of a plurality of processors enters data into a common storage area, interrupt

controllers associated with the processors detect the entry and send interrupt signals to the processors to initiate a synchronous job or to change the state of operation of the processors. (Reply Br. at 3.)

Kametani relates to synchronizing processors. Col. 1, ll. 20-22. Each of a plurality of processors $1n$, $1n+1$ is provided with a synchronous circuit unit $2n$, $2n+1$. The synchronous circuit units $2n$, $2n+1$ exchange data through signal lines 8. The synchronous circuit units $2n$, $2n+1$ each include a synchronous register 5 and a determination circuit 6. The synchronous register 5 stores data defining a group of the processors that perform related tasks. The determination circuit 6 compares exchanged data with the contents of the synchronous register 5. Col. 8, ll. 20-45.

Consider an example of establishing synchronization among processors $1n$ and $1n+1$ where a first processor $1n$ finishes its task first. Upon finishing, the first processor $1n$

stores a bit sequence in synchronous register 5. The bit sequence defines a processing group constituted by processors n and $n+1$. Bits n and $n+1$ of the sequence are set to logical "1"; the remaining bits, to logical "0". Simultaneously, a flip-flop 7 is triggered by an active pulse on a signal line 4. Consequently, the flip-flop 7 outputs a task termination signal set at logical "0" at its output terminal Q and a status signal set at logical "1" at its other output terminal. The task termination signal is coupled to the n th line of the signal lines 8 through which it is transferred to the synchronous circuit unit $2n+1$ of the other processor $1+n$. In addition, the status signal is supplied to a TEST input terminal of the first processor $1n$. The first processor $1n$ interrupts its processing until the status signal at the TEST input terminal is set to logical "0." Col. 9, ll. 1-24.

Values stored in the synchronous register 5 and those on the signal lines 8 are supplied to the determination circuit 6. When the n th and $(n+1)$ th lines of the signal lines 8 are set

to logical "0", a trigger signal 10 becomes active at logical "0". The flip-flop 7, in response to the active trigger signal 10, is preset. This sets the task termination signal and accordingly the nth line of the signal lines 8 to logical "1", which also sets the trigger signal 10 to logical "1". Simultaneously, the status signal at the output terminal Q is set to logical "0", setting the TEST input terminal of the first processor 1n also to logical "0", whereby the first processor 1n resumes its interrupted processing. The same operation is also performed in the other processor n+1, so that the processors 1n and 1n+1 are synchronized. Id. at ll. 24-48.

In short, Kametani teaches comparing the contents of the synchronous register 5 of a given synchronous circuit unit with data transmitted on the signal lines 8. Collectively, these data are a data set. The data set, however, does not reside in a common storage area as claimed. To the contrary, it resides on the signal lines 8.

The examiner has not identified anything in Kametani, Papadopoulos, or the prior art as a whole that would have suggested storing the data transmitted on Kametani's signal lines 8 in a common storage area. His aforementioned comment that the claim language does not indicate that the data set or common storage area is used to synchronize the processors evidences a failure to consider all the limitations of the two "wherein" clauses of claim 4 and the relationship therebetween. The examiner erred by focusing only on part of the first "wherein" clause.

For the foregoing reasons, the examiner failed to show that Kametani and Papadopoulos teach or would have suggested the "wherein" clauses of claim 4 and its dependent claims 5 and 6. Therefore, we find that the examiner's rejection does not amount to a prima facie case of obviousness. Because the examiner has not established a prima facie case, the rejection of claims 4-6 over Kametani in view of Papadopoulos is

improper. Therefore, we reverse the rejection of the claims under 35 U.S.C. § 103.

CONCLUSION

To summarize, the decision of the examiner to reject claims 4-6 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON)	
Administrative Patent Judge)	
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)	
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)	BOARD OF PATENT
JOHN C. MARTIN)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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