

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte IAIN C. ROBERTSON, JEFFREY L. NYE, MICHAEL D. ASAL,
GRAHAM B. SHORT, RICHARD D. SIMPSON and JAMES G. LITTLETON

Appeal No. 1997-4224
Application No. 08/474,866¹

ON BRIEF

Before URYNOWICZ, KRASS and JERRY SMITH, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

¹ Application for patent filed June 7, 1995. According to appellants, this application is a division of Application No. 08/359,324 filed December 15, 1994, now U.S. Patent No. 5,546,553 issued Aug. 13, 1996.

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This is a decision on appeal from the final rejection of claims 25 through 27, 53, 54, 59 and 68 through 76.

The invention is directed to a multifunctional access device and method. More particularly, an address translator receives an address supplied by an address bus of a first computer and outputs translated addresses to an address bus of a second computer. The address translator comprises a register having address segments and a control signal is provided responsive to detection that the address at address inputs changes from one segment to another segment.

Representative independent claim 25 is reproduced as follows:

25. A multifunction access circuit for use with first and second digital computers each having an address bus for addresses, the access circuit comprising:

an address translator circuit having address inputs for addresses supplied by the address bus of the first computer and outputs for translated addresses to the address bus of the second computer, the address translator circuit also having registers establishing address segments, said address translator circuit responsive to addresses on the address inputs is [sic, in] the address segments; and

control logic circuitry connected to said address translator circuit and operative to supply a control signal in response to detection that the address at the address inputs changes from one segment to another segment.

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The examiner relies on the following reference:

Schreiber	4,503,429	Mar.
5, 1985		

Claims 25 through 27, 53, 54, 59 and 68 through 76 stand rejected under 35 U.S.C. § 103 as unpatentable over Schreiber.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

We reverse.

It is the examiner's duty, in the first instance, to establish a case of prima facie obviousness when applying a rejection based on 35 U.S.C. § 103. In the instant case, while we do not determine that a prima facie case could not have been made in the instant case, based on the evidence provided by Schreiber, we merely conclude that the examiner simply has not done so.

The independent claims each call for, in one form or another, a first and second computer. The examiner has

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identified the two computers in Schreiber as the existing video board and the graphics board in Figure 3. Assuming, arguendo, that the examiner's interpretation is reasonable (the examiner has never explained why the video board and graphics board are considered to be "computers"), the instant independent claims further require that each computer has an address bus. Yet, the examiner only identifies, at column 12, line 40, and column 5, line 63, of Schreiber, a graphic processor having address and data buses. It is unclear how this translates into an address bus for each of the video board and the graphics board identified by the examiner as being two computers. Thus, it is unclear what, in Schreiber, the examiner relies on for the teaching or suggestion of two separate address buses.

Further, the instant independent claims call for an address translator having address inputs for addresses supplied by the first computer and outputs for translated addresses to the address bus of the second computer. While Schreiber discloses an address translator, at 420 in Figure 4, it is unclear how this address translator meets the claim language without the required two address buses. Moreover,

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the claims require the address translator to have registers establishing address segments and that control circuitry connected to the address translator supplies a control signal "in response to detection that the address at the address inputs changes from one segment to another segment."

Notwithstanding the examiner's contention that Schreiber discloses such a register establishing segments in line register 465, it is not clear, from the examiner's reasoning, why the storage of X and Y addresses in Schreiber, in order to specify a single location, is considered to teach or suggest the claimed registers establishing address segments which, when it is detected that an address at an address input changes from one segment to another, cause the supply of a control signal, as claimed. We find nothing in Schreiber regarding addresses at the address inputs changing from one segment to another segment, as required by the instant claims.

Since, in our view, the examiner has failed to set forth a prima facie case of obviousness through a convincing line of reasoning, we will not speculate as to the disclosure of the Schreiber patent and we will not sustain the rejection of

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claims 25 through 27, 53, 54, 59 and 68 through 76 under 35

U.S.C.

§ 103.

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The examiner's decision is reversed.

REVERSED

STANLEY M. URYNOWICZ, JR.)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
ERROL A. KRASS)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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