

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board

Paper No. 31

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte SCOTT SARNIKOWSKI, UNMESH AGARWALA,  
STANLEY S. QUAN, CHARLES E. COMSTOCK, and FRANK G. MOORE

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Appeal No. 1998-0706  
Application 08/166,279<sup>1</sup>

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ON BRIEF

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Before MARTIN, JERRY SMITH, and BARRY, Administrative Patent Judges.

MARTIN, Administrative Patent Judge.

**DECISION ON APPEAL**

This appeal was taken under 35 U.S.C. § 134 from the examiner's December 4, 1996, Office action finally rejecting claims 8, 12, 16-21, and 26-41, all of the pending claims. In the Answer, the examiner adhered to the rejections of only

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<sup>1</sup> Application filed December 13, 1993, as a continuation of Application 07/599,325, filed October 17, 1990 (abandoned).

claims 8, 12, 16, 17, 20, 26, 27 and 30-39 and objected to dependent claims 18, 19, 21, 28, 29, 40, and 41 as depending on rejected claims (Answer at 2).

We affirm-in-part and reverse-in-part.

**A. The invention**

The invention relates to communication between processors in a multiprocessor system which is made up of a plurality of groups of processors, the groups being connected in a ring configuration.

**B. The claims**

There are six independent claims before us, of which claims 16 and 17 are representative:

16. Apparatus for communicating messages between at least three multiprocessor groups, each of the multiprocessor groups including a plurality of processor units coupled to one another for interprocessor communication by an interprocessor bus, the messages including information identifying a one of the plurality of processor units of a one of the multiprocessor groups as a destination processor unit for receiving the message, the apparatus comprising:

each of the multiprocessor groups including interface means coupled to the interprocessor bus of that multiprocessor group for receiving messages communicated thereon by a processor unit of that multiprocessor group to the destination processor unit;

link means intercoupling the interface means of each multiprocessor group in a ring configuration for communicating data thereon;

the interface means of each of the multiprocessor groups including first circuit means for communicating all data received from the link means to the interprocessor bus in the form of a message, second circuit means for retrieving and storing messages communicated on the interprocessor bus having information identifying the destination processor unit as not being a one of the plurality of processor units of that multiprocessor group, and third circuit means for transmitting the messages from the second circuit means onto the link means in the form of data; and

configuration means for determining which processor unit is located with which multiprocessor group of processor units.

17. A multiprocessor system, comprising:
  - at least three processor sections, each of the processor sections containing a plurality of processor means;
  - link means interconnecting the three processor sections in a ring configuration for communicating data therebetween;
  - each of the processor sections including,
    - interprocessor bus means for communicating message data between the plurality of processor means, the message data having identification data indicative of a destination processor means of said message data;
    - data interconnect means having right and left data transfer means respectively coupled by the link means to each of the other of the three processor sections and to the interprocessor bus means for communicating message data between the plurality of processor means of said processor sections and the plurality of processor means of other of the three processor sections, the right and left data transfer means each respectively coupled to a one and another of the processor sections, and including routing table means containing information indicative of the processor section nearest the left or the right data transfer means.

### **C. The references and rejections**

The rejections before us are based on the following U.S. patents:

Allen et al. (Allen)	4,667,287	May 19, 1987
Bione et al. (Bione)	4,707,827	Nov. 17, 1987

Claims 8, 12, 16, and 30-39 stand rejected under 35 U.S.C. § 103(a) for obviousness over Allen.

Claims 17, 20, 26, and 27 stand rejected under 35 U.S.C. § 103(a) for obviousness over Allen in view of Bione.

**D. Appellants' burden of persuasion on appeal**

Appellants bear the burden of showing that the evidence on which the examiner relies is insufficient to establish a prima facie case of obviousness or that appellants have provided evidence which rebuts the prima face case of obviousness. See In re Rouffet, 149 F.3d 1350, 1355 47 USPQ2d 1453, 1455 (Fed. Cir. 1998):

To reject claims in an application under section 103, an examiner must show an un rebutted prima facie case of obviousness. See In re Deuel, 51 F.3d 1552, 1557, 34 USPQ2d 1210, 1214 (Fed. Cir. 1995). In the absence of a proper prima facie case of obviousness, an applicant who complies with the other statutory requirements is entitled to a patent. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). On appeal to the Board, an

applicant can overcome a rejection by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobviousness. See id.

Appellants challenge the sufficiency of the evidence on which the examiner's prima facie case is based.

**E. The merits of the § 103 rejection based on Allen alone**

Comparing claim 16 to Figure 3 of Allen, the examiner reads the claimed interprocessor bus means onto busses 12a-n, the claimed plurality of link means onto data links 22a-d and 24a-d, the claimed interface means onto cluster modules 18a-n. As for the claimed components of a cluster module (shown in Figure 4), the examiner reads the first means and third means onto cluster module controller 32 (col. 6, ll. 4-13) and reads the second means onto LEFT OUTQ BUFFER 40 and RIGHT OUTQ BUFFER 42. The examiner correctly concedes that Allen does not disclose having the first circuit means communicate all data received from the link means to the interprocessor means, as required by the claim. While Allen's cluster module temporarily stores all of the data received from the link means in buffer memory 34 (col. 8, ll. 25-35 and 48-52), the only stored data that is then passed on to local

interprocessor bus 12b is the data intended for one of the processors connected to that bus (col. 7, l. 54 to col. 8, l. 9). Stored data intended for a processor in another cluster is sent to the left or right adjacent cluster module 18 via data link 22, 24, 26, or 28 without first being coupled to the local interprocessor bus (col. 6, ll. 17-20 and 52-55).

The examiner contends it would have been obvious to modify Allen's cluster modules so that they communicate all data received by the data links to the local interprocessor bus 12b because "by placing all incoming data on the interprocessor bus and then examining it, the throughput of the system is improved by eliminating a step taken by the interface means" (Answer at 4). The examiner further explains (Answer at 8):

In both the Applicant's claimed invention and the system of Allen, the interface means is responsible for determining whether or not a message is destined for a processor in that group. By communicating all message data onto the interprocessor bus and then taking action, the complexity and cost of the system become reduced because the buffer then only stores the messages which are destined for processors that are not part of the present group.

These reasons are unconvincing because they lack any basis in Allen, the only reference cited in support of the rejection, which discloses communicating to the interprocessor bus only those messages which are intended for processors connected to that interprocessor bus. Nor can we treat the examiner's reasoning as stemming from the basic knowledge or common sense of the artisan. Cf. In re Zurko, \_\_\_ F.3d \_\_\_, \_\_\_ USPQ2d \_\_\_ (Fed. Cir. August 2, 2001), slip op. at 9-10:

[T]he deficiencies of the cited references cannot be remedied by the Board's general conclusions about what is "basic knowledge" or "common sense" to one of ordinary skill in the art. As described above, the Board contended that even if the cited UNIX and FILER2 references did not disclose a trusted path, "it is basic knowledge that communication in trusted environments is performed over trusted paths" and, moreover, verifying the trusted command in UNIX over a trusted path is "nothing more than good common sense." . . . We cannot accept these findings by the Board. This assessment of basic knowledge and common sense was not based on any evidence in the record and, therefore, lacks substantial evidence [sic] support. As an administrative tribunal, the Board clearly has expertise in the subject matter over which it exercises jurisdiction. This expertise may provide sufficient support for conclusions as to peripheral issues. With respect to core factual findings in a determination of patentability, however, the Board cannot simply reach conclusions based on its own understanding or experience -- or on its assessment of what would be basic knowledge or common sense. Rather, the Board must point to some concrete evidence in the record

in support of these findings. [Footnote omitted.] To hold otherwise would render the process of appellate review for substantial evidence on the record a meaningless exercise. Baltimore & Ohio R.R. Co. v. Aderdeen & Rockfish R.R. Co., 393 U.S. 87, 91-92 (1968) (rejecting a determination of the Interstate Commerce Commission with no support in the record, noting that if the Court were to conclude otherwise "[t]he requirement for administrative decisions based on substantial evidence and reasoned findings -- which alone make effective judicial review possible -- would become lost in the haze of so-called expertise"). Accordingly, we cannot accept the Board's unsupported assessment of the prior art.

Because the examiner has not provided adequate evidence of motivation for modifying Allen in the proposed manner, the rejection of claim 16 and its dependent claims 8 and 12 is reversed. For the same reasons, we are also reversing the rejection of independent claims 30-39, which is based on the same reasoning as the rejection of claims 8, 12, and 16.

**F. The merits of the § 103 rejection based on Allen and Bione**

The only limitation of claim 17 that is in dispute is the requirement that the data interconnect means, which corresponds to Allen's cluster modules, "includ[e] routing table means containing information indicative of the processor section nearest the left or the right data transfer means." Referring to appellants' Figure 6, the routing table register

206 includes a table (Fig. 8) made up of 1's and 0's indicating which of the two directions (i.e., left or right) provides the shorter path to each of the processors located in the other clusters (Specification at 30, ll. 8-12, and at 32, ll. 10-24).

As correctly noted by the examiner in the Answer at 9, Allen states that "[t]he network attempts to send the messages over the shortest possible route" (col. 1, ll. 67-68).<sup>2</sup> While Allen fails to explain how the shortest direction is determined, the examiner and appellants correctly agree that the direction determination is made in the sending processors rather than in the sending cluster modules as required to satisfy the claim. Specifically, when data is to be sent from a processor in one cluster to a processor in another cluster, the processor issues a SEND instruction (col. 9, ll. 36-44). Parameters supplied to the SEND instruction include, inter alia, the identity of the direction in which the packet is to be sent around the ring, the identity of the receiving cluster module, and the identity of the receiving processor within the

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<sup>2</sup> Appellants' opening brief does not address this passage in Allen. Nor did they file a reply brief.

multiprocessor system connected to the receiving cluster module (id. at ll. 44-51). The cluster module of the sending processor notes the selected direction and replaces the routing information with the number of the sending cluster:

If the packet is destined for a processor within a different cluster, the sender cluster number contains routing information. The cluster module, in turn, examines the routing information, determines which direction the packet should be sent from this information, and then replaces the routing information with the sender cluster number. [Col. 9, ll. 56-62.]

If a processor, having sent a transmission, fails to receive an acknowledgment within a specified time interval, software in the sending processor will send the transmission again and then wait once more for the specified time interval, with the successive transmissions being switched through the two cluster modules and through both of the possible directions around the ring (col. 10, ll. 35-43). Thus, if any one of the four possible paths from a processor to another processor is functioning correctly, the message can be transmitted (col. 10, ll. 43-46).

Bione is cited by the examiner as evidence that it would have been obvious to move the direction determination function

from Allen's processors to Allen's cluster modules (Answer at 10). Specifically, the examiner relies on the following description in Bione of a prior art communication system that employs look-up tables to effect communication between the stations of different LANs:

LANs using the same protocol are interconnected by a control interface referred to as a "bridge".

Prior art bridge interfaces commonly comprise so-called memory look-up tables for providing a cross-reference between each station connected to the bridge interface (bridge) and the LAN in which the respective station is situated. More particularly, the memory look-up tables are used to store a plurality of addresses, each identifying a respective station, together with a code identifying the particular LAN to which the station belongs. When a message is directed via the bridge to a given destination station, the memory look-up table is searched to locate the stored address code of the destination station for determining the LAN to which the station belongs. For stations in LANs serviced by different bridges, an interbridge address is created and put in temporary memory when the message is forwarded to the next bridge. The process is repeated for each message, with the bridge directing

the message to the appropriate LAN for receipt by the destination station. [Col. 1, ll. 18-38.<sup>3</sup>]

Citing the foregoing passage, the examiner argues (for the first in the Answer at 10) that "[i]t would have been obvious to replace the decision making of the individual processors with routing table means that are included in the data interconnect means because a more central location for a routing table eliminates the need for distributed tables, thus decreasing the overall cost of the system." Appellants did not file a reply brief specifically addressing this reasoning. Furthermore, appellants' sole argument in their opening brief in opposition to the proposed combination of Allen and Bione, i.e., that "Bione fails to teach, or even suggest, a 'routing table means containing information indicative of the processor section nearest . . . [a] left or . . . right data transfer

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<sup>3</sup> Bione, after explaining that "[w]hile the foregoing procedure normally operates satisfactorily, the use of such look-up tables and interbridge addresses to effect communications between stations of different LANs is hardware intensive and therefore a relatively costly as well as a low-speed technique" (col. 1, ll. 41-46), discloses a system which operates in a different manner. Appellants do not contend that Bione considered as a whole teaches away from using look-up tables in the bridge interfaces.

means.' (claim 17, line[s] 23-26)" (Brief at 15) fails to address the examiner's reliance on Allen's disclosure of selecting the shortest path (col. 1, ll. 67-68).

In view of appellants' failure to demonstrate any error in the rejection of claim 17, we are affirming the rejection of that claim.

Independent claim 20 recites that the interconnect means includes routing table means for identifying the shortest route to a destination processor. Appellants, after correctly noting that the decision about direction is made in Allen's individual processors, argues that "adding a routing table to Allen's cluster module adds nothing (and for this reason, Applicants submit, the motivation to combine Allen with Bione is not suggested by either Allen or Bione)" (Brief at 15). This "adds nothing" argument is unconvincing because it misconstrues the examiner's position to be that it would have been obvious to add a direction-determining capability to Allen's cluster modules without removing that capability from the individual processors. The examiner has instead proposed to move that capability from the individual processors to the cluster modules in order to reduce the number of distributed

routing tables. Because appellants have not shown any error in the examiner's reasoning, the rejection of claim 20 is affirmed.

As the foregoing unconvincing argument is appellants' sole argument with respect to claim 26 and dependent claim 27, the rejection of those claims is also affirmed.

**G. Summary**

In summary, the rejection of claims 8, 12, 16, and 30-39 is reversed and the rejection of claims 17, 20, 26, and 27 is affirmed.

Appeal No. 1998-0706  
Application 08/166,279

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

**AFFIRMED-IN-PART; REVERSED-IN-PART**

JOHN C. MARTIN	)
Administrative Patent Judge	)
	) BOARD OF PATENT
	)
	) APPEALS AND
JERRY SMITH	)
Administrative Patent Judge	) INTERFERENCES
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	)
LANCE LEONARD BARRY	)
Administrative Patent Judge	)

JCM/sld

Appeal No. 1998-0706  
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